An Investigation of Photovoltaic Power Optimization

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ABSTRACT

This work is concerned with the effects of low frequency switching with a non-linear step size DC-to-AC direct conversion on systems that employ photovoltaic (PV) power as an input source. These techniques exhibit dramatic reductions in circuit complexity and power dissipation compared to traditional pure sine-wave inverters. However, designing multilevel DC-to-AC inverter-less systems with maximum efficiency and reduced circuit complexity is challenging. This project has produced two novel multilevel DC-to-AC inverter-less systems for PV applications that reduces the power dissipation and circuit complexity to minimum.

First, a DC-to-AC direct conversion system based on two ladders of switches structured as in the Golomb ruler is implemented at 600 Hz switching frequency. The technique has been evaluated analytically, experimentally and by simulation. The evaluation prove the reduction in series resistance loss of Golomb structure over the conventional contiguous block arrangement. It is also shown that Golomb structure

can cause uneven PV panel utilization.

In order to ensure even panel utilization and produce a good-quality sine-wave output signal, a novel cyclic selection multilevel inverter-less system is developed. The need for the magnetic materials is removed by selecting series and parallel combinations of PV cells. Closed-form cyclic selection expressions are derived and analytically investigated. Calculations prove that this system has exactly the same performance as a conventional magnetic core-based inverter. Laboratory and simulation results prove the efficiency of the system in PV applications.

The task of determining the timing steps of the multilevel signal of known amplitude is resolved using a completely new mathematical method to minimize harmonic distortion. Closed-form expressions for the timing steps method are derived for three levels signal and the methodology is extended to an unlimited number of levels. This method gives the same results as the well-known Fourier series method but requires no carefully-chosen optimization starting point.

Finally, a multiple step, forward-backward algorithm is employed to maximize the power into a given load. This work uses the second order central difference theory to establish an approximate equation for MPPT. This approach is unlike previous work in that it does not rely on a PV side tracking. Laboratory and simulation results prove the efficiency of the algorithm in rapidly varying insolation conditions.

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Acronyms and Abbreviations

DC	Direct Current
AC	Alternating Current
PV	Photovoltaic
MPPT	Maximum Power Point Tracking
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
LED	Light Emitting Diode
CO2	Carbon Dioxide
ppmv	parts per million per volume (moles per million per volume)
GW	gigawatt
GWp	gigawatt peak
TWh	terawatt hour
EU	Europe
Hi - Ren	High Renewable (Scenario)
ETP	Energy Technology Perspectives
Gt	gigtonnes
Mt	Million tonnes
OECD	Organization for Economic Co-operation
PO	Perturbation & Observation
MPP	Maximum Power Point
VMPP	Voltage of Maximum Power Point
IncCond	Incremental Conductance
NS	Negative Small

NB	Negative Big
ZE	Zero
PS	Positive Small
PB	Positive Big
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
THD	Total Harmonic Distortion
MSEV	Mean Square Error Voltage
TD	Total Distortion
FFT	Fast Fourier Transform
RMS	Root Mean Square

CHAPTER 1

INTRODUCTION

1.1 Motivation

Significant research efforts have been focusing on the development and quality enhancement of the photovoltaic (PV) direct current to alternating current (DC-to-AC) inverters. Starting with the identification of design goals, the PV power inverter designers have to propose viable solutions based on reduced circuit complexity and current technological impediments. A particular challenge in this aspect is to pin down the optimal compromise between design complexity, power maximization, high efficiency, and cost. This work investigates the impact of direct conversion multilevel

(DC-to-AC) circuits on PV applications. One of the major advantages of multilevel design is the reduction of the output waveform harmonic distortion without increasing the switching frequency.

In recent years, a rising number of multilevel inverter topologies have been used for PV applications to overcome the circuit complexity of the conventional pure sine-wave inverters. These include, neutral point-clamped (diode clamped) [1–3], flying capacitor [4, 5] and cascaded H-bridge [6, 7] amongst others. These configurations employ a large number of active and passive components (examples being switching devices (MOSFETs or transistors), diodes, capacitors and inductors). The issue of power dissipation in solar inverters, due to capacitors, inductors and solar cell resistance for example, has been considered in recent years. One way to reduce the power dissipation in the system and improve the efficiency of the conversion is to use low frequency switching inverters with a non-linear step size such as DC-to-AC multilevel inverters.

Direct conversion multilevel topologies for PV applications using switching techniques have emerged recently, in many cases outperforming the conventional pure sine-wave and multilevel inverters in terms of circuit complexity. However, conventional pure sine-wave inverters emerge a competitive performance in terms of high efficiency and full source utilization for high power PV applications.

New challenges arise in the requirements of maximum power point tracking (MPPT) design, as a result of the mismatch between the PV power source and the load. Previously, several MPPT methods have been studied and presented such as direct control open circuit voltage [8, 9] and short circuit current [10] methods. One of the major disadvantages of the existing methods is that the power is maximized at the PV side.

This is accounted as a drawback due to the fact that a lossy DC-to-DC converter stage between the PV and the load can cause a failure in delivering the maximum power.

The work in this thesis was delivered in the context of a wider project that focused on exploring and experimenting with two different direct conversion DC-to-AC multilevel topologies for PV applications. A Simulink PV model was developed in this work to validate the proposed MPPT algorithm. In the present study, the Simulink simulator is only used for the purpose of validating the proposed theoretical analyses, whenever possible.

It is noteworthy that all the resulting contributions of this thesis are not confined to the low power context. They are of much wider interest and could find application in high power systems in general.

1.2 Contributions of The Thesis

The objective of this thesis is to present DC-to-AC multilevel direct conversion systems suitable for PV applications. Two novel DC-to-AC, staircase, inverter-less topologies are presented and their applicability are experimentally demonstrated. The conversion techniques are suitable for PV applications. A novel MPPT algorithm is presented and validated by experiment and simulation. A new mathematical method of determining the timing steps of multilevel signals of known amplitude is determined and experimentally attempted.

To the author's knowledge, the following aspects of the thesis are believed to be novel contributions:

1. Golomb Multilevel DC-to-AC Inverter

   The concept of staircase inverters in PV applications is not new, but here for the first time it is believed, a direct conversion multilevel DC-to-AC system at low frequency for PV applications is attempted. The structure of this inverter is based on the Golomb-ruler number theorems.

2. Cyclic Selection Multilevel DC-to-AC Inverter

   The novelty in the cyclic selection scheme is the concept of implementing direct conversion DC-to-AC multilevel topology for on-panel battery provision. In addition, the use of a cyclic selection algorithm to select cell voltage and ensure even panel utilization adds further value to the originality of this scheme.

3. Multilevel Signals Timing Steps Optimization

   A completely new mathematical method based on a mean square-error voltage approach for determining the timing of the multilevel signals of known amplitude is theoretically derived and empirically evaluated in the control algorithm of the cyclic selection DC-to-AC topology.

4. Multiple Step, load-side Power Maximization

   Although the concept of MPPT is not new, in this study, a new MPPT algorithm based on a multiple steps central difference scheme is attempted. Moreover, maximizing the power into any given load under various insolation levels further adds to the novelty of the scheme. In this scheme, a simple heuristic, but accurate, PV model is used in Simulink to evaluate the algorithm.

1.3 Structure of the Thesis

This thesis is organized as following:

Chapter 2 constitutes an overview of the existing MPPT techniques and multilevel inverters for PV applications. Two major existing MPPT control methods, direct and indirect, are described at length.

Chapter 3 describes a direct conversion DC-to-AC Golomb staircase topology and explains the various steps involved in its design. A brief review of Golomb rulers is also included. MATLAB simulation of the optimum Golomb ruler deficiency is also explained. The principles of operation and the control technique are presented in detail followed by the evaluation of Golomb topology in terms of power losses. An overview of the experimental setup is then given including the characteristics of the major components. The Simulink simulation and experimental results of the six-level Golomb ruler inverter are also presented in this chapter.

Chapter 4 presents a direct conversion DC-to-AC cyclic selection multilevel topology for PV applications. A mathematical analysis of the cyclic selection algorithm with its major classifications is described at length. A new innovation of a modular Golomb-Sparse-Wichmann ruler is also discussed and compared to the existing modular Golomb and sparse rulers. The principles of operation and the control technique of the proposed topology are described in detail followed by its performance comparisons with a conventional PWM inverter. The design of the experimental setup and the characteristics of the major components are also explained. This chapter also includes the Simulink simulation and experimental results of the seven-level cyclic se-

lection inverter. The overall performance of the Golomb ruler and the cyclic selection systems is compared and the differences between them are explained.

Chapter 5 presents the mathematical analysis of the timing steps of the multilevel signals optimization method and the multiple step, forward-backward algorithm. The principles of operation and an overview of the experimental setup of the MPPT optimizer are also described. The construction of the solar simulator is explained in detail followed by the characteristics of its major components, namely, PV panel and LED floodlight. This chapter also discusses the simulation and experimental results of the multiple step, forward-backward optimizer.

Chapter 6 concludes the present thesis and presents suggestions for further research on the same topics.

CHAPTER 2

OVERVIEW OF SOLAR POWER

2.1 Introduction

Traditional power sources, in particular fossil fuels, have significant and harmful impacts on the environment due to the increase on greenhouse gas concentrations, air quality deterioration, water pollution and acid precipitation. The energy demand and economic growth are increasing as the global population growth rate increases. In fact, the total energy demand is projected to grow by an average of 1% per year between 2010 and 2040 [11]. A more substantial effort is needed to minimize the atmospheric concentrations of greenhouse gases and carbon dioxide CO_2, and their

negative impacts on global warming and climate change. Since the beginning of industrialization era, there is evidence that the atmospheric CO_2 concentration is increasing significantly from its pre-industrial value of approximately 280 ppmv to over 400 ppmv at present [12, 13]. Alternatives to toxic power sources are becoming desirable if not essential to replace carbon-intensive power sources and limit global warming emissions. Renewable power sources are considered to be environmentally friendly and can harness natural processes. Therefore, renewable sources are becoming a substantial part in electricity generation in the entire planet. Solar photovoltaic (PV) remains the third most important renewable energy source, after hydro and wind power, with a total of 70 GW global installed capacity in 2011 and about 139 GW, 177 GW and 227 GW installed in 2013, 2014 and 2015 respectively [14, 15]. This shows a significant potential for PV resource in electric generation capacity for the globe. Solar power has a number of benefits compared to conventional power generation:

- It is a non-carbon-dioxide power source and generates no greenhouse emissions, although during PV fabrication greenhouse gas emission is generated.
- The fuel (Sun) is free.
- The utility-scale-solar power plants are easy to assemble and disassemble, contributing positively to the economy and rural electrification.

The global photovoltaic market continued to grow from 38 GW added in 2013 to approximately 40 GW added in 2014, in contrast to an about 32.3% drop in the European market (declined from approximately 9.92 GWp in 2013 to only 6.88 GWp

in 2014) [14, 16]. About 80.2 TWh were generated by photovoltaic power system in 2013 with only 11.1 TWh growth in 2014, the latter covered approximately 6% of the EU′s peak electricity demand in 2014 [16–18]. According to the Global Market Outlook report 2014, the installed PV capacity in Europe is expected to be between 119 GW and 156 GW by 2018 and target up to $\sim$ 10% and 15% of the electricity demand by 2030 with respect to baseline and accelerated scenarios respectively [18]. The PV power will consequently lead to a global de-carbonization and EU CO_2 emissions mitigation. For instance, based on the high-renewables scenario (hi-Ren) of ETP 2014, the PV power would avoid approximately 4 Gt (gigatonnes) of carbon dioxide CO_2 on an annual basis for 4 600 GW worldwide installed capacity by 2050 [19]. By contrast, the deployed PV systems at the end of 2013 have generated 160 TWh/year and avoided approximately 140 Mt (Million tonnes) of CO_2 per year. Following the hi-Ren scenario, the deployment of PV in OECD Europe would avoid 2% CO_2 emission of the total global installed capacity by 2050. Over the next 35 years, the PV CO_2 mitigations would equal wind power with respect to the hi-Ren scenario 2014 [19].

This chapter presents a general overview of the previous well-cited work of the Maximum Power Point Tracking (MPPT) techniques and the available multilevel inverters for photovoltaic applications as shown in section 2.2 and section 2.3 respectively.

2.2 A Review of MPPT Techniques

In photovoltaic power applications, (MPPT) systems are employed to match the variation of the voltage and current I-V characteristics of the solar panels with a

given load. From the typical non-linear I-V curve, the PV module produces a small amount of current as the output voltage increases as shown in Figure in 2.1.

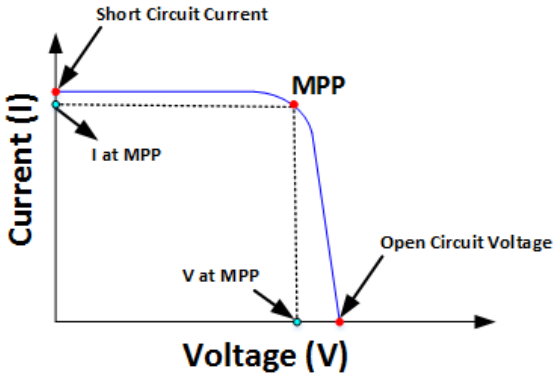

Figure 2.1: Solar cell I-V curve

The optimal operating point (MPP) of PV arrays is needed to be found to increase the efficiency of PV power generators. This is however a challenging task due to the fact that the I-V characteristics of the PV panels depends mainly on the solar irradiance level. In fact, the PV module operates effectively on bright days with no blockage to the incident sunlight. Partial obstacles such as trees and large buildings limit the availability and efficiency of solar power in domestic and industrial suburbs. Thus, tracking the MPP of PV modules is an important part of any power generation system to eliminate the mismatch between solar panels and a given load. Generally, the (MPPT) is classified into two main categories: the first method is based on matching the characteristics of any given load to the PV MPP's while the second is using an intermediate matching circuit between the load and the PV module [20, 21].

The first form is a direct connection of the DC-load to the PV source. The theoretical perfect matching would occur if the load characteristics (V_L, I_L) and the PV characteristics (V_{PV}, I_{PV}) are identical [22]. It has been indicated in the literature that

this technique is applied mainly to DC motors where the motor characteristics are designed to operate at the PV MPP′s or close to it [22]. The main disadvantage of this method is the fact that it is very challenging to manufacture a perfect load that matches the PV system due to the non-linear behaviour of the PV module. Another drawback of this technique is that it is only appropriate for certain loads such as batteries and DC motors.

The second form of the MPPT is using a matching circuit between the supply source and the load. This is generally achieved by a DC-to-DC converter such as a buck converter, boost converter and, buck - boost converter [23–26]. To control these intermediate stage power conversion, many MPPT algorithms have been developed which are detailed in section 2.2.1. Figure 2.2 illustrates various MPPT classifications and methods.

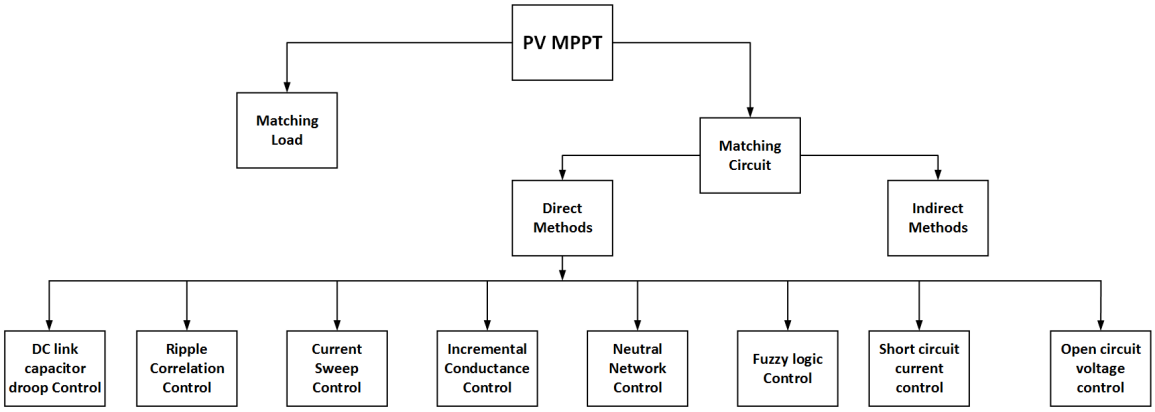

Figure 2.2: The classifications of MPPT techniques

2.2.1 Direct MPPT Control

This method is based on algorithms that use PV array parameters such as voltage, current, insolation level, power and temperature.

2.2.1.1 Hill Climbing & Perturb and Observe (PO)

These algorithms are the most used techniques in the PV generation systems due to their simple implementation [27]. The hill climbing method [28], requires a perturbation in the duty ratio of the power converter while the PO method involves perturbation in the operating voltage of the PV array [28]. In the case of the hill climbing method, perturbing the duty ratio of power converter leads to the PV current perturbation and the latter perturbs the PV array voltage as a consequence [28]. Figure 2.3 shows that the power increases on the left of the MPP as the voltage increases, whereas the power decreases on the right of MPP as long as the voltage increases. The perturbation direction should be kept the same to reach the MPP if there is an increase in the PV output power. However, if there is a decrement in the PV output power the perturbation direction should be reversed [28]. Table 2.1 summarizes the operating principle of the PO and hill climbing techniques.

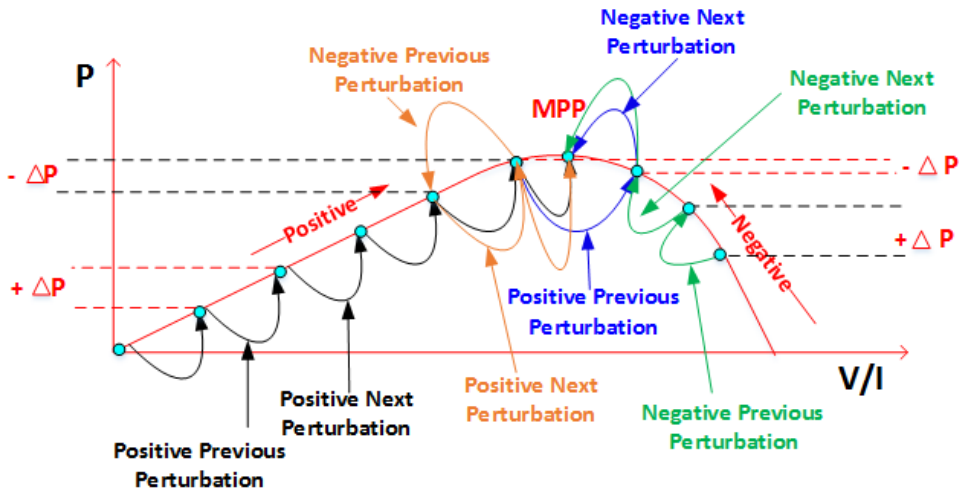

Figure 2.3: PO and Hill climbing algorithms

Table 2.1: The operating principles of PO and hill climbing techniques

Previous Perturbation	Change in Output Power	Next Perturbation
Positive	Positive	Positive
Negative	Negative	Positive
Positive	Negative	Negative
Negative	Positive	Negative

It can be concluded, from Table 2.1, that the next perturbation direction is the product of both directions of the previous perturbation and the output power. The process of perturbation and reversing the direction is repeated periodically until the MPP is reached. The system is oscillating around the MPP and it can be reduced by decreasing the size of the perturbation step. However, minimizing the perturbation step size slows down the MPPT. To overcome this problem, a variable perturbation step size is used which becomes smaller to reach MPP [29,30]. D'Souza, et al. (2005) showed that the PO and hill climbing algorithms work also with instantaneous PV array current and voltage as the sampling occurs once in each switching cycle [31].

However, the PO and the hill climbing methods can fail when the weather condition changes rapidly. If there was a sudden change in the weather condition, for example a sudden drop in the irradiance from point A to point B as shown in Figure 2.4. This figure shows that a decrease in irradiance condition causes a drop in the power level, which is not caused by the change in the voltage. Therefore, the PO and the hill climbing algorithms will fail to track the MPP because the algorithm will reduce the voltage in the wrong direction that lead to more power dissipation and losses. To overcome this problem and ensure the tracking of the MPP even with a sudden change in irradiance, many methods can be applied [29–32]. In [32], three-point weight comparison PO method is used to avoid the oscillation problem. In the three-point weight comparison method, a perturbation sign decision is not made until the actual power point compared to only two proceeding ones [32]. However, the sampling rate is optimized to overcome the irradiance problem [30]; while in [29] toggling is made between the conventional hill climbing method and a modified hill climbing method to avoid the diverging from the MPP. Further, a high sampling rate technique is applied to prevent the deviation from the MPP [31].

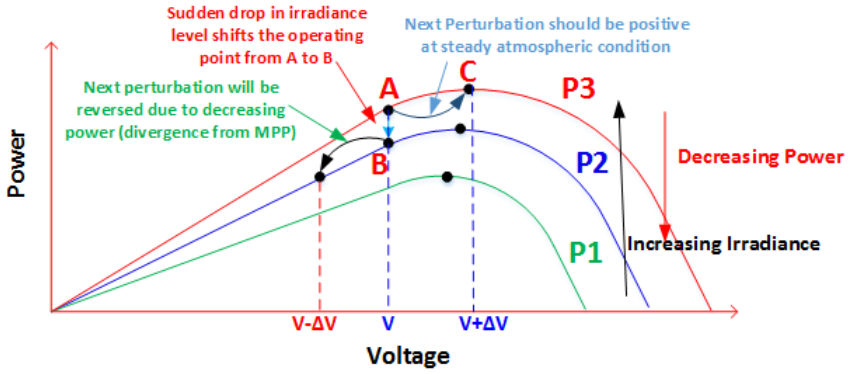

Figure 2.4: Divergence of hill climbing and PO from MPP

2.2.1.2 Incremental Conductance

Incremental conductance (IncCond) is another direct control MPPT technique [28]. The method is mainly based on the slope P - V curve that equals zero at MPP and it is positive in the left and negative at the right as shown in Figure 2.5.

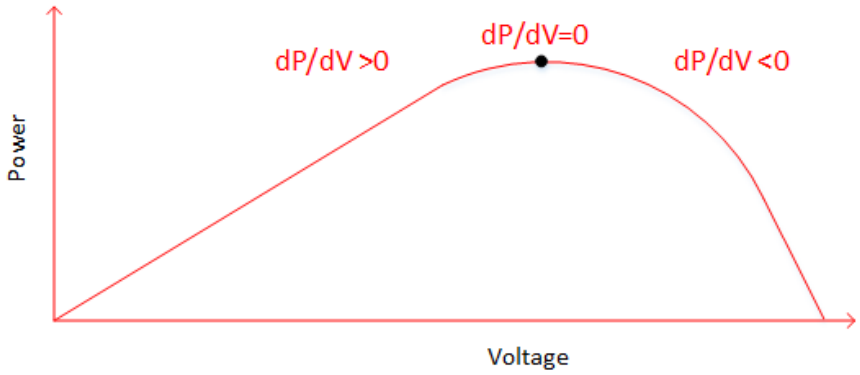

Figure 2.5: The P-V curve for the incremental conductance method

The principle of the incremental inductance method can be summarized as follows:

$$\frac{\mathrm{I}}{\mathrm{V}} > -\frac{\mathrm{d}I}{\mathrm{d}V} \quad \text{For} \quad \frac{\mathrm{d}P}{\mathrm{d}V} > 0 \tag{2.1}$$

$$\frac{\mathrm{I}}{\mathrm{V}} < -\frac{\mathrm{d}I}{\mathrm{d}V} \quad \text{For} \quad \frac{\mathrm{d}P}{\mathrm{d}V} < 0 \tag{2.2}$$

$$\frac{\mathrm{I}}{\mathrm{V}} = -\frac{\mathrm{d}I}{\mathrm{d}V} \quad \text{For} \quad \frac{\mathrm{d}P}{\mathrm{d}V} = 0 \tag{2.3}$$

The direction of the perturbation is determined by the relation between I/V and dI/dV. The IncCond method identifies whether the MPP is reached or not. The perturbation stops when the MPP is reached and it runs again when the relation between I/V and dI/dV is not equal [33]. The incremental conductance method has an advantage over the PO and hill climbing methods. IncCond calculates the

perturbation with changing the voltage and it tracks the MPP with high accuracy when the weather condition is varying [28]. However, the incremental conductance method requires more calculations, resulting in slowing the speed of the sampling rate [33]. This method not only it slows down the sampling rate speed but also requires more sensors to measure the current and voltage.

2.2.1.3 Open - Circuit Voltage Control

An open circuit voltage ratio technique is another MPPT method that arises from the fact that the voltage at the maximum power point is approximately the same under varying irradiance and temperature levels as illustrated in Figure 2.6 below. The relationship between the open circuit voltage of the PV array and the MPP voltage is approximately linear under changing weather conditions (irradiance and temperature levels). The constant voltage method is well-cited in the literature [8, 10, 34].

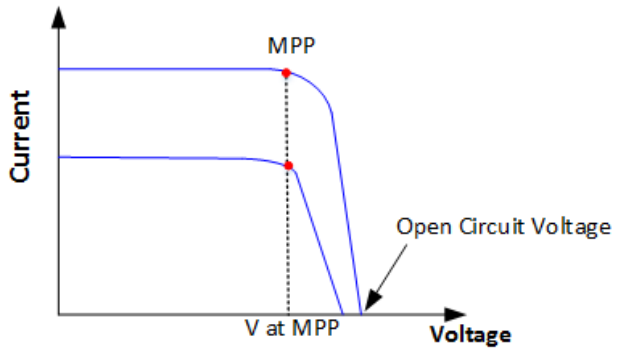

Figure 2.6: The I-V curve for the fractional open circuit voltage method

The MPP voltage (VMPP) is a fraction of the open circuit voltage as described in equation (2.4).

$$V_{MPP} \approx k_1 \times V_{OC}, \tag{2.4}$$

where k_1 is a constant which illustrates the proportionality relation between the open circuit voltage V_{OC} and the MPP voltage V_{MPP}. This means that k_1 depends on the PV array characteristics and can be calculated in advance at variant irradiance and temperature conditions. The constant k_1 has been reported to be in the range of 0.72 - 0.78 [10]. Given k_1, V_{MPP} can be determined using equation (2.4) where the open circuit voltage is measured periodically. This can be done by shutting the power converter momentarily to obtain the open circuit voltage [28]. One drawback of this technique is the temporal power loss caused by shutting the power converter to measure the open circuit voltage. This method is based on an estimated value and thus the PV array technically does not operate at the MPP. The accuracy of this technique is further reduced by temperature variation of the solar cells which significantly affects the open circuit voltage [33]. Furthermore, when the PV array is partially shaded, k_1 in equation (2.4) is no more valid due to two maxima [28]. However, this method is cost effective, easy to implement and fast in allocating the MPP.

2.2.1.4 Short - Circuit Current Control

The fractional short circuit current I_{SC} method rises from the fact that the current at the MPP I_{MPP} is a fraction of the short circuit current I_{SC} under changing weather conditions as illustrated in equation (2.5).

$$I_{MPP} \approx k_2 \times I_{SC} \tag{2.5}$$

In this case, k_2 is the ratio between the short circuit current and the MPP current. This parameter is reported to be in the range of 0.75 - 0.92 [10]. Measuring the short circuit current is difficult. An additional switch is needed in the power converter to short circuit the PV array periodically and measure the current using a current sensor [28]. In contrast with the other mentioned methods, this technique has many disadvantages including circuit complexity (requires more components) and, expense. In addition, with this method, the MPP is just an estimate which means that the system never operates at the exact MPP. However, this method is easy to implement and efficient in some applications such as battery charging and street lighting.

2.2.1.5 Fuzzy Logic Method

One of the well-known data-based method is the fuzzy logic control technique. The fuzzy logic method is a microcontroller based algorithm which has three stages: fuzzification, rule base table lookup, and de-fuzzification [28]. The fuzzification period involves converting numerical input variables to linguistic variables based on membership functions as shown in Figure 2.7.

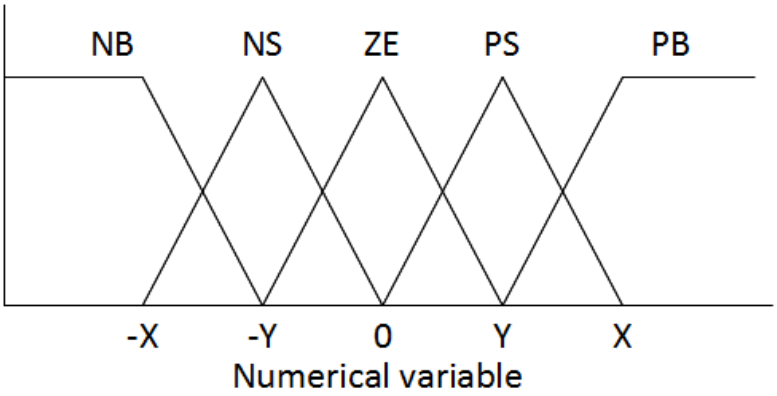

Figure 2.7: The membership function of fuzzy logic inputs and outputs

Figure 2.7 shows five fuzzy levels: NS (negative small), NB (negative big), ZE (zero), PS (positive small) and PB (positive big). The inputs to a logic fuzzy controller are normally an error E and a change in error $\triangle E$ [28]. It is shown in section 2.2.1.2 that dP/dV vanishes at the MPP and thus in turn the MPP is found. Following the fuzzy logic approach in [35], the variable E (Fuzzy logic error) and $\triangle E$ (Fuzzy logic change in error) can be written as in equations (2.6) and (2.7) respectively.

$$E(n) = \frac{P(n) - P(n-1)}{V(n) - V(n-1)} \tag{2.6}$$

$$\triangle E(n) = E(n) - E(n-1) \tag{2.7}$$

The equations can be computed in different ways for user's flexibilities and choices. The output of the fuzzy logic controller can be looked up in the rule-based table once E and $\triangle E$ are found and converted to the linguistic variables. The logic controller output is a change in the duty ratio of the power converter $\triangle D$ [35]. The linguistic variables of $\triangle D$ for various combinations of E and $\triangle E$ rely on the knowledge of the users and also on the power converter being employed. For instance, if the operating

point is far to the left of the MPP in Figure 2.3, which indicates that E is PB and $\triangle E$ is ZE as shown in the rule-based table based on a boost converter Table 2.2 [28]. The duty ratio of the power converter $\triangle D$ should be PB to reach the MPP.

Table 2.2: Fuzzy logic rule-based table based on a boost converter

$\triangle E$ / E	NB	NS	ZE	PS	PB
NB	ZE	ZE	NB	NB	NB
NS	ZE	ZE	NS	NS	NS
ZE	NS	ZE	ZE	ZE	PS
PS	PS	PS	PS	ZE	ZE
PB	PB	PB	PB	ZE	ZE

After finishing stage one and two, the linguistic variables $\triangle D$ are converted to numerical variables using the membership function illustrated in Figure 2.7. This analogue signal controls the power converter to reach the MPP [35]. This method keeps tracking the MPP under varying weather conditions. This technique works directly with the inputs with no need for the accurate mathematical equations. However, this method depends on the knowledge of the user on choosing the right fuzzy logic range and producing the rule-based table [28].

2.2.1.6 Neural Network Method

A neural network is one of the direct MPPT methods, which is similar to fuzzy logic as both are using a microcontroller. This method consists of three types of layers or possibly more: input, hidden and output layers as illustrated in Figure 2.8.

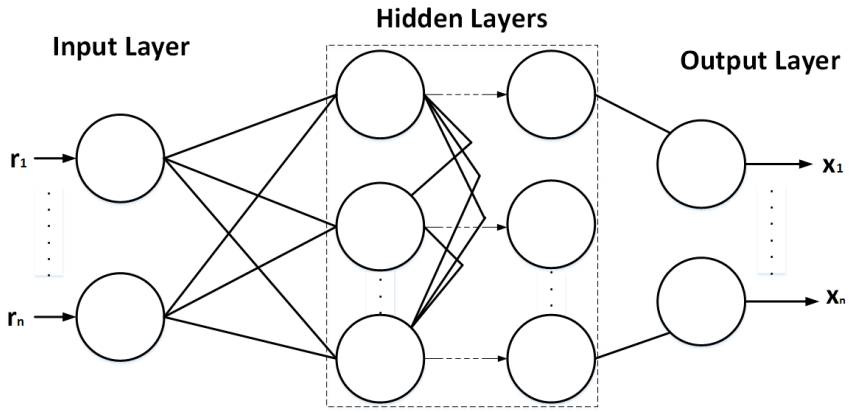

Figure 2.8: Neural network structure

The input variables can be PV array parameters (open circuit voltage, short circuit current), weather parameters (irradiance, temperature) or the combination of both PV and atmospheric parameters. The output is typically one or more reference signals such as a duty cycle signal that allows the power converter to work close to the MPP [28]. The algorithm used by the hidden layer will show how close the operating point gets to the MPP and how well the neural network has been trained [28]. The main drawback of this method is that the network has to be trained periodically to obtain accurate results due to the variation in weather conditions.

2.2.1.7 Ripple Correlation Control RCC

Besides the previous direct methods there is another maximum power point technique that makes use of the voltage and current ripple of the PV array. This method is a ripple correlation control RCC which correlates the time derivative of the time varying PV array voltage or current with the time derivative of the time varying power to drive the power gradient to zero and reach the MPP [28]. Unlike other methods, this

method is cost effective and easy to implement the RCC circuit. The method does not require prior knowledge of the PV array parameters.

2.2.1.8 Current Sweep Control

A current sweep [36] is one of the commonly used methods in tracking the maximum power point MPP which uses a sweep waveform for the current of the PV array. For instance, the I - V characteristic of the used PV array is measured and updated at fixed periods of time. MPP can be calculated at the same periods. The function used by this technique is proportional to its derivative as illustrated in equation (2.8) [28].

$$f(t) = k\frac{df(t)}{d(t)}, \tag{2.8}$$

where k is a constant. The power of the PV array is given by equation (2.9)

$$p(t) = v(t)i(t) = v(t)f(t), \tag{2.9}$$

where p(t), v(t), i(t) are the instantaneous values of power, voltage and current of the PV array, respectively.

At the MPP:

$$\frac{dp(t)}{dt} = v(t)\frac{df(t)}{dt} + f(t)\frac{dv(t)}{dt} = 0 \tag{2.10}$$

Substituting (2.8) to equation (2.10), we get

$$\frac{dp(t)}{dt} = [v(t) + k\frac{dv(t)}{dt}]\frac{df(t)}{dt} = 0 \tag{2.11}$$

Thus:

$$f(t) = D\exp(t/k) \tag{2.12}$$

where D is chosen to be the maximum current of the used PV array I_{max} , k is to be negative, resulting in a decreasing exponential function with a time constant of τ=-k. Equation (2.12) leads to equation (2.13)

$$f(t) = I_{max}\exp(-t/\tau) \tag{2.13}$$

The current in equation (2.13) can be simply found by using a discharging circuit through a capacitor as an example. The derivative of (2.13) is not vanishing, thus it is possible to divide both sides of equation (2.11) by df(t)/dt as in (2.14).

$$\frac{dp(t)}{di(t)} = v(t) + k\frac{dv(t)}{dt} = 0 \tag{2.14}$$

So once the voltage at MPP is found, equation (2.14) can be applied to check whether the MPP has been reached or not. This method is only practical when the power consumption of the tracking system is lower than the increase in power that it can bring to the entire PV system [28]. This method is more complex in comparison to earlier techniques and it requires two sensors. However, the maximum power point tracked by this technique is not an estimate unlike the fractional open circuit voltage and short circuit current methods [28].

2.2.1.9 DC Link Capacitor Droop Control

DC link capacitor droop control [37, 38] is a special technique that is used to track the maximum power point of the PV system. This technique is specifically designed to work with a PV system connected in parallel with an AC unit as shown in Figure 2.9.

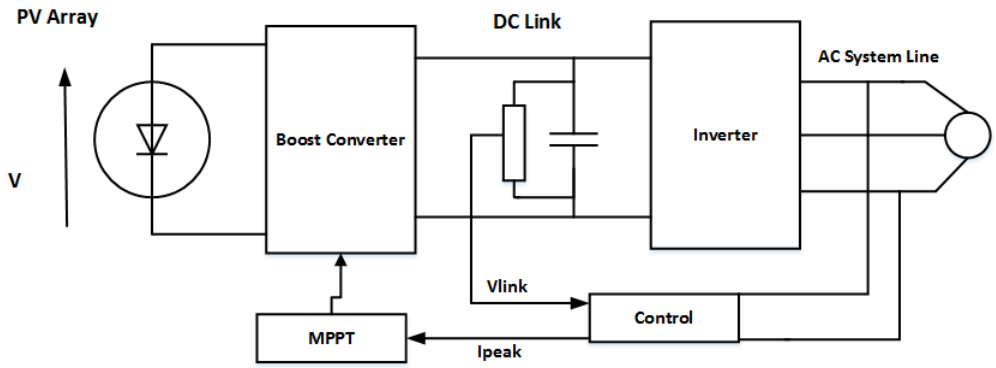

Figure 2.9: The circuit topology for DC link capacitor droop control

The duty ratio of a boost converter is given by equation (2.15)

$$d = 1 - \frac{v}{v_{link}}, \tag{2.15}$$

where v is the array voltage; and v_{link} is the voltage across the DC link. When the voltage of the DC link is kept constant, the current going to the inverter is increasing. The latter increases the power out of the boost converter and thus increases the power out of the used PV array [37]. As long as the required power by the inverter does not exceed the maximum power available by the used PV array, v_{link} is kept constant while the current is rising. If this is not true, the DC link voltage starts drooping. Before that point, the used PV array operates at the MPP and the current control command

of the inverter is at maximum. To prevent the DC link voltage from drooping, the AC system line current is fed back and the duty ratio is optimized to maximize I_{peak} and thus reach the MPP [37]. This method does not require the computation of PV power, but according to [38], its response deteriorates due to the fact that its response depends directly on the DC voltage control loop of the inverter.

2.2.2 Indirect MPPT Control

This method is based on the fractional open circuit and short circuit methods, but the measurements are made on a small solar cell known as a pilot cell. This pilot cell has the same characteristics as the other cells in the PV array. The pilot cell measurement is used by the MPPT to track the MPP of the solar array [28]. This reduces the power loss during the open circuit voltage and short circuit current measurements. The characteristics of the pilot cell are significantly affected by weather parameters such as the temperature and irradiance level. The main drawback of this method is the fact that matching the characteristic of the PV array by pilot cell are not guaranteed due to rapidly varying weather conditions.

2.3 Multilevel Inverter for PV Applications

A high performance direct current (DC) to alternating current (AC) inverter is currently an essential component of the solar electrical power generation. In general, inverters can be categorized as: pure sine-wave, square wave, modified square wave

and multilevel. The multilevel topology is generally more attractive than the others due to lower switching losses [39,40] and reduced total harmonic distortion compared to square wave inverters [41]. Many industrial applications require a high power level, and medium voltage such as motor drive systems and the utility grid. As it is difficult to connect only one power switch directly in a medium voltage grid situation, multilevel inverters have been found to solve the problem [42]. Multilevel inverters can in fact achieve high power rating and allow the use of renewable energy sources such as PV and wind. These environmentally friendly sources can be easily interfaced with multilevel inverters [43–45]. Of particular interest here are inverters for PV applications and advanced switching topologies.

The idea of multilevel inverters was first found in 1975 and the first topology consisted of three levels [42]. Moreover, a number of multilevel topologies with different levels has been documented in [46,47]. In [46], a single phase, five-level multilevel inverter with a full bridge transformer-less network was presented. The switches of this topology operate such that zero, +E, +2E, -E and -2E output levels are generated. A bidirectional current is permitted to flow between the load and the bridge inverter at all times due to the arrangement of the diodes [46]. This eliminates the voltage spiking and the waveform distortion caused by changing in the polarity between the levels in the output waveform. However, reference [48] documented a multilevel inverter associated with a three phase AC motor at which a PWM control technique was used to vary the speed of a medium voltage motor. The bridge inverter could be more efficient than the PWM control technique as the latter includes transformers which are expensive. The switching technique mentioned in [46] is more attractive than the PWM method in [48] due to low switching frequency and low power dissipation [42].

Multilevel inverters can in fact generate an output voltage with low distortion and low voltage stresses at high efficiency [42], thus minimizing the electromagnetic interference (EMI) [49]. In general, there are three main structures of multilevel inverters that have been used in different applications: cascaded H-bridge, Diode clamped and Flying capacitor multilevel inverters as illustrated in Figure 2.10.

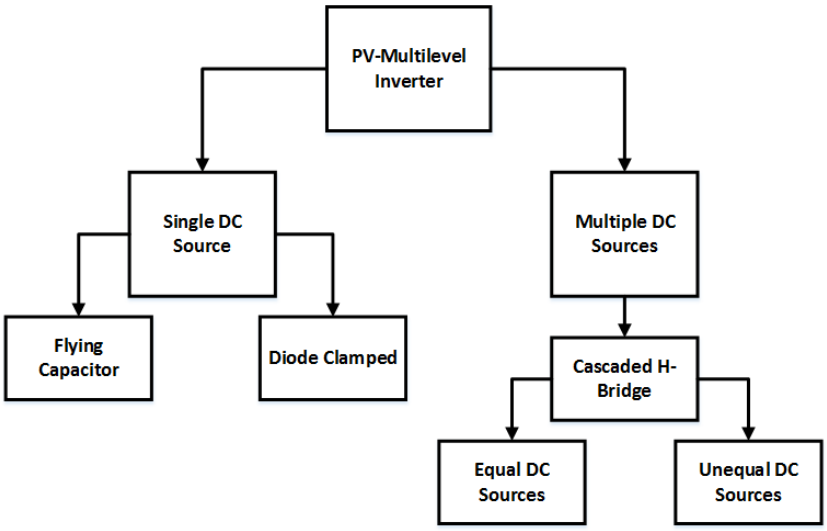

Figure 2.10: The general classification of multilevel inverters

The first diode clamped structure (neutral point clamped) of three levels was found by Nabae, Takahashi, and Akagi in 1981 as shown in Figure 2.11. This topology utilizes a bank of capacitors to split the DC bus voltage. Four, five and six-level diode clamped inverters were documented in 1990s and applied to various applications, such as static var compensation and high voltage system interconnections [50–53].

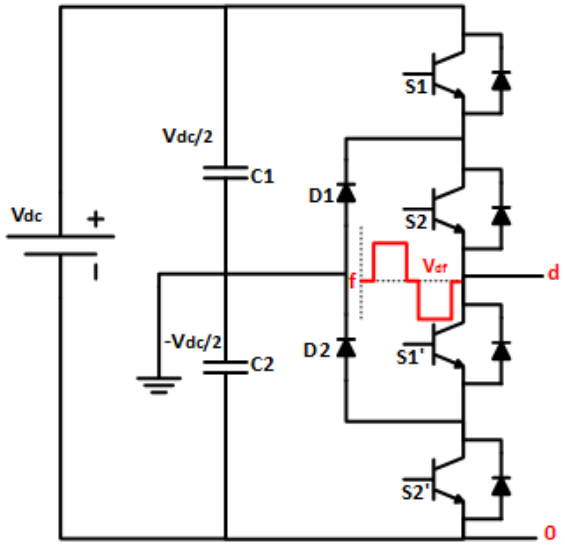

Figure 2.11: Three-level diode clamped multilevel inverter circuit topology

This topology has a number of advantages such as the capacitors can be pre-charged as a group. In addition, with this structure, a common DC line is shared between the phases in the three phase topology to minimize the requirement of capacitors [42]. However, for a single inverter the real power flow is very difficult due to the overcharge and discharge of the intermediate DC levels [39,42]. This topology has overcharge and discharge issues. Moreover, it has no isolated inputs or outputs [42]. Furthermore, the number of diodes of this topology increases quadratically with the number of levels [39]. A few attempts of standalone and grid tie photovoltaic applications of diode clamped inverters were reported in [44,54]. This topology becomes very difficult when the number of levels increases due to the requirement of clamped diodes and the significant issues of isolating the DC sources.

The flying capacitor topology was introduced in 1992 by Foch and Meynard [42]. This topology is similar to the neutral point clamped except that the clamped diodes

are replaced with capacitors [49] as shown in the three level example in Figure 2.12. The output voltage levels of this topology can be generated by different combinations of switching states contrasted by the neutral point clamped where the output levels are limited to just one switching state. Flying capacitor inverters increase flexibility on choosing both the output voltage levels and switches to discharge and charge the capacitors [42, 55]. However, the control of this inverter is complex and requires a large number of capacitors. The flying capacitor and diode clamped topologies are both bulky and expensive [42].

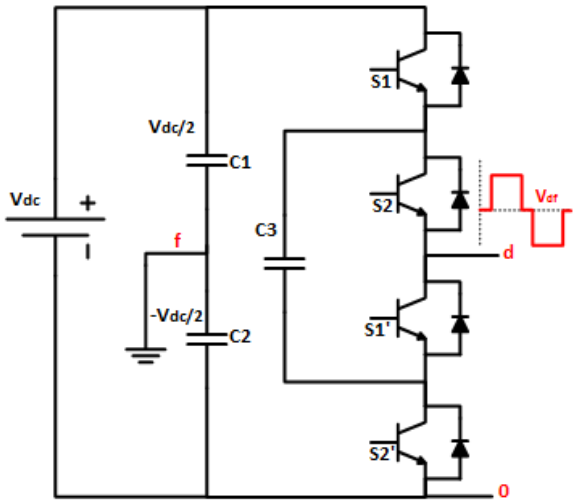

Figure 2.12: Three-level flying capacitor multilevel inverter circuit topology

Cascaded H-bridge inverters have been used for different applications such as the static var generation, battery-based applications and the interface with the renewable sources [42, 43]. Three different structures of H-bridge inverters are found in literature, being bi-directional DC-to-DC cascaded topology, transformer-less and multiple transformers topologies. The transformer-less inverter has multiple sources contrasted by the multiple transformers topology where only one source connected to

a full bridge circuit followed by several low frequency transformers before the load. The bi-directional DC-to-DC inverter operates at a high frequency mode and requires only one DC source [42].

The cascaded H-bridge is an attractive topology in photovoltaic applications due to its modular and ease of control [42], [56, 57]. Furthermore, this topology employs low rating power semiconductors compared with the two-level topology [56]. Other authors consider diode clamped multilevel inverters for photovoltaic applications to be more attractive than cascaded H-bridge inverters due to lower count of active power devices per PV array and ease of implementation [43]. Cascaded multilevel inverters can be extended to three phases with minimum circuit complexity unlike diode clamped inverters where the required clamped diodes increase quadratically with the number of levels and thus the number of phases.

Multilevel inverters have several advantages over conventional pure sine-wave configurations, for example, multilevel topology features a number of DC links which allows individual controlling and tracking of the different PV arrays [56]. In addition, multilevel inverters provide a high quality voltage waveform with switches operate at a frequency near the fundamental and thus lower output harmonic and lower commutation losses [42]. For this topology to compete the standard two-level PWM converters, cost and overall configuration complexity (at both power and modular circuits) have to be minimized. To overcome these issues, simplified multilevel inverters using advanced switching techniques should be employed, however, these have attracted less attention in literature. An attempt of a simplified 15-level multilevel inverter have been reported in [58]. The latter consists of two main parts: a level and a full H-

bridge module. This reduces the layout complexity and minimizes the required power switches by about 75% when compared to the multilevel inverters [59–61]. However, the power sources in [58] are not evenly utilized. In [62], a simplified five-level H-bridge inverter is implemented using an H-bridge circuit, two capacitors as voltage dividers and auxiliary circuit of four diodes and a controlled switch. This configuration has increased the required diodes to four times higher (8 instead of 2) when compared with the five-level diode clamped configuration presented in [63]. However, the topologies presented in [62] and [63] has reduced the number of required diodes to 60% (8 instead of 20) and 90% (2 instead of 20) respectively when compared to conventional five-level diode clamped inverter documented in [64].

A comparison of eight different single-phase, seven-level multilevel inverters with various configurations is presented in Table 2.3.

Table 2.3: Comparison between eight different seven-level multilevel topologies

Configuration	Switches	Diodes	Capacitors	DC sources
Cascaded H-Bridge [65]	12	-	-	3
Cascaded H-Bridge [66]	12	12	-	3
Flying capacitor [67]	6	-	3	1
Diode clamped [65]	12	10	6	1
Cascaded Level module multilevel inverter [58]	6	2	-	2
Flying Capacitor based Active Neutral Point Clamped [68]	10	-	4	1
Proposed Multilevel inverter in [69]	8	8	-	3
Cascaded Active Neutral Point Clamped (ANPC) [70]	10	10	3	1

It can be concluded from Table 2.3 that the configuration proposed in [58] minimizes the required number of power switches by 50% when compared with the seven-level cascaded H-bridge inverters presented in [66] and [65]. The cascaded level module multilevel inverter has further reduced the required number of diodes to approximately 83.3% and 80% when compared to the cascaded H-bridge configuration in [66] and the diode clamped in [65], respectively. The number of the required DC sources in the

cascaded level module multilevel inverter is also reduced when compared to cascaded H-bridge inverters in [66] and [65]. The multilevel inverters documented in [65] and [70] require 10 diodes to form a seven-level output signal while only two diodes are required in the configuration proposed in [58]. The topology proposed in [58] has completely eliminated the requirement for capacitors. This leads to 100% reduction in the number of capacitors when compared to the inverters proposed in [65], [67] and [70].

2.4 Conclusion

The maximum power point tracking techniques, introduced above, are widely used in PV power applications but their performance fail under rapidly varying irradiance conditions, solutions to which are challenging but not impossible. The drawbacks of the direct MPPT techniques were almost overwhelming in the past due to cost differences compared to indirect control. The indirect techniques were rarely used due to mismatches between the pilot cells and the PV array. However, the direct tracking methods such as the OP and the hill climbing still fail under various insolation levels. Multilevel inverters are the preferable technique to interface with PV sources due to reduction in the commutation loss. The multilevel configuration layout, on the other hand, is complex and requires a large number of power switches which increases dramatically with the number of output levels. Cascaded level module multilevel inverter is an excellent configuration in reducing circuit complexity but the energy of the PV source is inefficiently utilized.

In the next chapters, a load side MPPT technique is presented that can track and find the MPP at various insolation levels. Direct conversion multilevel systems based on the Golomb ruler and cyclic selection algorithm as optimization tools are also presented.

CHAPTER 3

GOLOMB RULER MULTILEVEL INVERTER

3.1 Introduction

It has been seen in the previous chapter that conventional multilevel inverters have a bulky design due to the need for semiconductor and passive components such as capacitors, diodes and switches. The number of these components is increasing dramatically as the number of output levels rises. In the seven-level diode clamped circuit topology proposed in [65], 12 switches, 10 diodes and 6 capacitors are required

while the flying capacitor topology reported in [67], 6 switches and 3 capacitors are needed for the same number of levels. It is also shown in the previous chapter that the classical seven-level cascaded H-bridge inverter requires 12 switches and 12 diodes. All of these inverters rely on series-connected panel installations and high switching frequency. The series-connected installations requires high-voltage inverters which have high switching losses. An advance switching topology such as a cascaded level module proposed in [58] has given a solution to the circuit complexity. However, this topology relies on a high switching frequency control method and hence high switching losses. The direct switching of PV cells to produce a useful AC waveform in a mathematically optimal sense has not been considered.

In this chapter, a new intrinsically-optimized, single-phase DC-to-AC staircase inverter based on the previously defined Golomb number theorems for photovoltaic applications is described. Golomb arrangement allows individual panel outputs to be aggregated in an optimal fashion to produce an approximate 50 Hz sine - wave output signal. Here, the third-order Golomb ruler ($\{0, 1, 3\}$) is chosen to realize a basic, but non-trivial, switched-cell arrangement for low power applications. The third-order Golomb ruler is used for realization purposes.

The main advantage of the Golomb structure over the conventional contiguous block arrangement is that it provides %36 less resistance loss and runs at the order of 1000 times lower frequency; hence virtually eliminating switching losses.

Implementing the single-phase Golomb inverter gives the low frequency switching advantage and minimizes both circuit complexity and power dissipation when compared with the conventional inverters. The ability to switch at a low frequency makes the

technique suitable for photovoltaic applications.

3.2 Golomb Rulers

Golomb rulers are named after Professor Solomon W. Golomb of the University of Southern California [71, 72]. This ruler can be defined as a ruler that has unevenly spaced marks at integer positions such that the space between any two marks is unique so it is fundamentally different from a normal ruler [73, 74]. The Golomb ruler was first used by Babock under a different name to overcome the problem of interference between radio communication channels [71]. Babock eliminated the third harmonic by assigning the frequencies of the channels to the marks of Golomb ruler. Despite the fact that Babock was the first who used Golomb ruler, it is named after Golomb who generated a systematic approach to the theory. The Golomb ruler can be defined formally by a set of integer numbers which are known as marks. The set of integers can be written as [71]:

$$F_x = \{\alpha_1, \alpha_2, ..., \alpha_n\} \qquad \alpha_1 < \alpha_2 < .. < \alpha_n \tag{3.1}$$

This set is called a Golomb ruler if for each integer $A \neq 0$ there is only one solution to the following equation

$$A = \alpha_i - \alpha_j \quad \alpha_i, \alpha_j \in F_x \tag{3.2}$$

There are two types of Golomb ruler: perfect Golomb rulers and optimal Golomb rulers. The perfect variety which allows all increments to be obtained with a minimum number of marks (but only up to 4^{th} order with 6 increments) as in the ex-

ample shown in Figure 3.1. The ruler $\{0, 1, 4, 6\}$ is a perfect ruler because it can measure the distances $\{1, 2, 3, 4, 5, 6\}$. However, the optimal ruler (presently up to 27^{th} order with 553 increments) misses out certain increments as in the example depicted in Figure 3.2. The ruler $\{0, 1, 4, 9, 11\}$ can only measure the following distances $\{0, 1, 2, 3, 4, 5, 7, 8, 9, 10, 11\}$.

Figure 3.1: Fourth order perfect Golomb ruler

Figure 3.2: Fifth order optimal Golomb ruler

Golomb rulers have the ability to measure exactly D distances with n marks (order). The difference between any two marks of a Golomb ruler is called a distance and the number of distances that a Golomb ruler can measure is given in equation (3.3):

$$D = \frac{1}{2}n(n-1) \tag{3.3}$$

Table 3.1 shows examples of the number of measured distances (D) of Golomb rulers of $(1 \leq \text{n} \leq 6)$ orders.

Table 3.1: The number of measured distances of Golomb Rulers of $1 \leq n \leq 6$

Order (n)	Golomb Ruler	D
1	$\{0\}$	0
2	$\{0, 1\}$	1
3	$\{0, 1, 3\}$	3
4	$\{0, 1, 4, 6\}$	6
5	$\{0, 1, 4, 9, 11\}$	10
6	$\{0, 1, 4, 10, 12, 17\}$	15

It is shown in the table above that beyond the perfect fourth order ruler all Golomb rulers are optimal.

Golomb rulers have been used in many applications such as radio astronomy and coding theory. Additionally, they have been applied under different names such as the distinct difference set and time hopping patterns [71]. Astronomers place different telescopes in a single line to measure electromagnetic radiation from a distant star, the difference of the measurements between two telescopes is taken at the same time to extract more information than single observation [71]. To maximize the pairwise distances, telescopes are placed at the marks of the Golomb ruler [71].

Golomb rulers have attracted the attention of many researchers because of their unique patterns. Some researchers have used different techniques to find a Golomb property in an array that is generated by a genetic search with a level decision of chromosome [75] where the difference between any two positions of ones in the array is distinct. For example, the 4×4 array shown in Table 3.2 has the Golomb property of the optimal variety because of the unique patterns between any two pairs of ones [75].

Table 3.2: Four by Four Optimal Array

1	1	0	1
1	0	0	0
0	0	1	0
1	0	0	0

The 4 × 4 array elements can be written in terms of their positions as follows:

Table 3.3: The location of the elements in the 4 × 4 optimal array

(1,1)	(1,2)	(1,3)	(1,4)
(2,1)	(2,2)	(2,3)	(2,4)
(3,1)	(3,2)	(3,3)	(3,4)
(4,1)	(4,2)	(4,3)	(4,4)

The unique patterns between any pair of ones in terms of their positions in table 3.3 is analyzed as a vector triangle as follows:

$$(0,1)(0,2)(1,-3)(1,2)(1,-2) \tag{3.4}$$

$$(0,3)(1,-1)(2,-1)(2,0) \tag{3.5}$$

$$(1,0)(2,1)(3,-3) \tag{3.6}$$

$$(2,2)(3,-1) \tag{3.7}$$

$$(3,0) \tag{3.8}$$

It is shown from the vector triangle above that the 4 × 4 array has the Golomb property as the distance (d_1, d_2) between any two pairs of ones is unique. According to [76], the triangle Golomb vector can be transformed as:

$$D(2) = [2N_1 - 1]d_1 + d_2 \tag{3.9}$$

Given $N_1 = 4$ in the 4×4 array example leads to:

$$D(2) = 7d_1 + d_2 \tag{3.10}$$

Thus, the vector triangle in (3.4) to (3.8) is transformed to (3.11)-(3.15) by using (3.10):

$$1 \quad 2 \quad 4 \quad 9 \quad 5 \tag{3.11}$$

$$3 \quad 6 \quad 13 \quad 14 \tag{3.12}$$

$$7 \quad 15 \quad 18 \tag{3.13}$$

$$16 \quad 20 \tag{3.14}$$

$$21 \tag{3.15}$$

The above transformation corresponds to a one dimensional Golomb ruler with six marks and all possible increments. The maximum possible of D(2) is 24 which can be found when the ones are poisoned at the opposite ends of the main diagonal, this means that (d_1, d_2) should be (3, 3) [76]. The above Golomb ruler is an optimum type ruler because of the fact that few distances can not be measured such as 10, 11, 12, 17. The one dimensional Golomb arrays have been used in the precise optical timing of pendulum clocks [76].

3.3 Deficiency of Optimum Golomb Rulers

The deficiency of an optimum Golomb ruler with n number of marks is the percentage of missing distances from the total length of the ruler. Section 3.2 showed that the Golomb ruler can measure exactly (D) distances without duplicating. The longest optimum Golomb ruler has a length of 553 and 27 marks at the positions 0, 3, 15, 41, 66, 95, 97, 106, 142, 152, 220, 221, 225, 242, 295, 330, 338, 354, 382, 388, 402, 415, 486, 504, 523, 546 and 553. This ruler measures exactly 351 distances, however, it is short by 202 of the total 553. This shows that the exact missing and available distances in the higher order optimal rulers are very challenging problem to be found manually.

In this section, a MATLAB algorithm of the deficiency of optimum rulers in percentage and the exact missing and measured distances is described. The reason of this initial step is to identify the deficiency of Golomb rulers as the order increases. In addition, this step will provide an automatic generation of both the exact missing and measured distances of any given optimum Golomb rulers. In some cases, the interest not only in counting the measured distances which are well defined by equation (3.3) but also in determining the exact missing and measured increments which are still not given in literature.

The algorithm description of any optimum Golomb ruler (G) is expressed in mathematical forms as follows:

$$G = \{a_1, a_2, a_3, ...a_n\} \tag{3.16}$$

where $a_1, a_2, ..., a_n$ are Golomb marks. Determining the binomial coefficients of a

Golomb ruler (G) by taking two marks at a time is presented in equation (3.17).

$$\begin{aligned} K &= C(G,2) \\ &= \{(a_l, a_{l+1}), (a_l, a_{l+2}), (a_l, a_{l+4}), ..., (a_{n-1}, a_n)\} \\ &= \{A_l, A_{l+1}, A_{l+2}, A_{l+3}, ..., A_{n-1}, A_n\} \end{aligned} \tag{3.17}$$

where K is the set of binomial coefficients of any pair of Golomb marks without duplicating them $(a_l, a_{l+1}), (a_l, a_{l+2}), ., (a_{n-1}, a_n)$. K has exactly $\binom{n}{2} = \frac{n!}{2!(n-2)!}$ maximum elements, where n is the order of the ruler.

To satisfy the definition of the Golomb ruler, a subtraction of the combinations between any two marks $(a_1, a_{l+1}), (a_l, a_{l+2}), (a_l, a_{l+3}), ..., (a_{(n-1)}, a_n)$ is applied and equated in (3.18):

$$H = \{(a_{i+1} - a_i), (a_{i+2} - a_i), (a_{i+4} - a_i), ..., (a_n - a_{(i+n-1)})\} \tag{3.18}$$

Sorting the elements in H in ascending order to find the measured increments g_s of an optimum Golomb ruler as in equation (3.19):

$$g_s = sort(H) = \{B_l, B_{l+1}, B_{l+2}, ..., B_n\} \tag{3.19}$$

To find the missing distances (m) in any optimum Golomb ruler (G), a comparison between (g_s) ruler and (F) ruler is determined, where F is a conventional ruler given in equation (3.20) with the same length (a_n) as G.

$$F = \{1, 2, 3, ..., max(G)\} \tag{3.20}$$

Finally, the deficiency of an optimum Golomb ruler is found by equation (3.21).

$$Deficiency = \frac{M}{M+D} * 100 \quad \% \tag{3.21}$$

where M is the number of missing distances, D is the number of measured distances as previously given in equation (3.3).

The detailed mathematical equations are evaluated in MATLAB (included on a CD) to generate the missing, measured distances, and the deficiency in percentage (%) for any given optimum Golomb ruler. Table 3.4 illustrates examples of the missing and measured distances of Golomb rulers of ($2 \leq$ n ≤ 7) orders and their deficiencies.

Table 3.4: Deficiency of Golomb Rulers of $2 \leq n \leq 7$

Order (n)	Ruler	Missing Increments (m)	Measured Increments (a)	Deficiency in %
2	[0 1]	None	1	0
3	[0 1 3]	None	1, 2, 3	0
4	[0 1 4 6]	None	1,2,3,4,5,6	0
5	[0 1 4 9 11]	6	1,2,3,4,5,7,8,9,10,11	9.0909
6	[0 1 4 10 12 17]	14,15	1,2,3,4,5,6,7,8,9,10,11,12,13,16,17	11.7647
7	[0 2 3 10 16 21 25]	12,17,20,24	1,2,3,4,5,6,7,8,9, 10,11,13,14,15,16,18,19,21,22,23,25	16

It is noticeable from Table 3.4 that the perfect Golomb rulers have zero deficiencies and all distances between the endpoints occur. However, the deficiency of optimum Golomb rulers is increasing in an unprecedented manner with the order (n) as shown in Table 3.5 and Figure 3.3. For instance, the deficiency of the fifth order ruler is approximately 9%, however, it is about 36.5% with 27^{th} order.

Table 3.5: Deficiency of Golomb Rulers of $8 \leq n \leq 27$

Order (n)	Ruler	(M)	(D)	Deficiency (%)
8	[0 1 4 9 15 22 32 34]	6	28	17.6471
9	[0 1 5 12 25 27 35 41 44]	8	36	18.1818
10	[0 1 6 10 23 26 34 41 53 55]	10	45	18.1818
11	[0 1 4 13 28 33 47 54 64 70 72]	17	55	23.6111
12	[0 2 6 24 29 40 43 55 68 75 76 85]	19	66	22.3529
13	[0 2 5 25 37 43 59 70 85 89 98 99 106]	28	78	26.4151
14	[0 4 6 20 35 52 59 77 78 86 89 99 122 127]	36	91	28.3465
15	[0 4 20 30 57 59 62 76 100 111 123 136 144 145 151]	46	105	30.4636
16	[0 1 4 11 26 32 56 68 76 115 117 134 150 163 168 177]	57	120	32.2034
17	[0 5 7 17 52 56 67 80 81 100 122 138 159 165 168 191 199]	63	136	31.6583
18	[0 2 10 22 53 56 82 83 89 98 130 148 153 167 188 192 205 216]	63	153	29.1667
19	[0 1 8 11 68 77 94 116 121 156 158 179 194 208 212 228 240 253 259 283]	93	190	32.8622
20	[0 1 8 11 68 77 94 116 121 156 158 179 194 208 212 228 240 253 259 283]	93	190	32.8622
21	[0 2 24 56 77 82 83 95 129 144 179 186 195 255 265 285 293 296 310 329 333]	123	210	36.9369
22	[0 1 9 14 43 70 106 122 124 128 159 179 204 223 253 263 270 291 330 341 353 356]	125	231	35.1124
23	[0 3 7 17 61 66 91 99 114 159 171 199 200 226 235 246 277 316 329 348 350 366 372]	119	253	31.9892
24	[0 9 33 37 38 97 122 129 140 142 152 191 205 208 252 278 286 326 332 353 368 384 403 425]	149	276	35.0588
25	[0 12 29 39 72 91 146 157 160 161 166 191 207 214 258 290 316 354 372 394 396 431 459 467 480]	180	300	37.5000
26	[0 1 33 83 104 110 124 163 185 200 203 249 251 258 314 318 343 356 386 430 440 456 464 475 487 492]	167	325	33.9431
27	[0 3 15 41 66 95 97 106 142 152 220 221 225 242 295 330 338 354 382 388 402 415 486 504 523 546 553]	202	351	36.5280

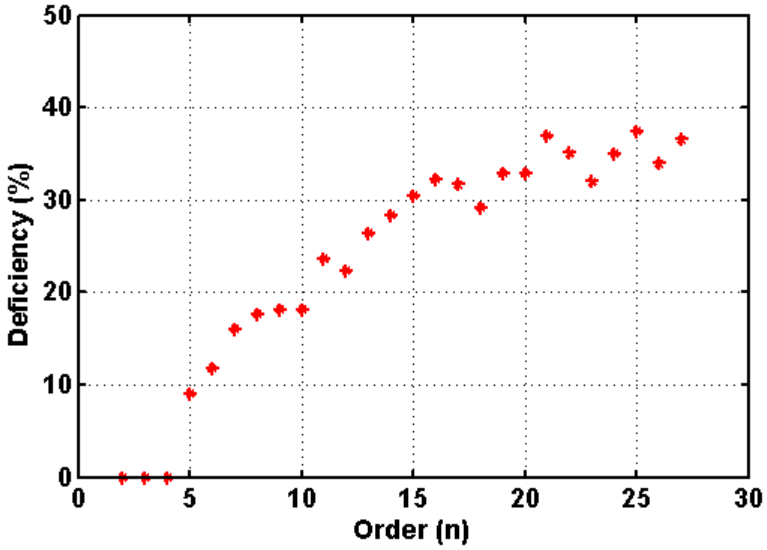

Figure 3.3: Deficiency of Golomb Rulers

The most striking feature of Figure 3.3 is the increasing deficiency of the optimum Golomb rulers with the order due to the fact that it is not possible to construct a higher order optimal Golomb with few missing increments. This indicates that the number of missing distances increases with the order. For instance, Golomb ruler

of 26^{th} order has a length of 492 and can measure 325 distances without repeating any increment. However, this is short by 167 of the 492 distances measurable by a conventional ruler of the same length.

3.4 A Multilevel DC-to-AC Golomb Inverter for Photovoltaic Application

3.4.1 The Operation Principle of a Single-Phase, Six-Level, Golomb Inverter

This section explains the principle of the proposed DC-to-AC Golomb inverter for a 6-level, single-phase structure without incorporating (zero level). However, the topology can be easily adapted to any number of levels (L) according to the order of Golomb ruler. The equivalent circuit of the third-order Golomb inverter structure is given in Figure 3.4. This topology consists of two ladders of bidirectional switches. The first ladder (positive rail), includes S_1, S_3 and S_5. The second ladder (negative rail), includes S_2, S_4 and S_6. These switches are connected to three identical DC sources (PV modules) (V_{dc1}, V_{dc2}, V_{dc3}) such that a third-order Golomb ruler is realized, hence, the steps between all voltage levels are equal. In fact, the number of switches connect to V_{dc1} (one DC source) is equal to the number of switches connected to V_{dc2} and V_{dc3} as depicted in Figures 3.5 and 3.6, respectively. The main advantage of this structure compared with the conventional contiguous block arrangement is that it provides 36% less series resistance loss and runs at the order of 1000 times lower frequency; hence

virtually eliminating switching losses. A notable reduction in the required number of power switches is another advantage of this new topology compared with other multilevel inverters of the same number of levels.

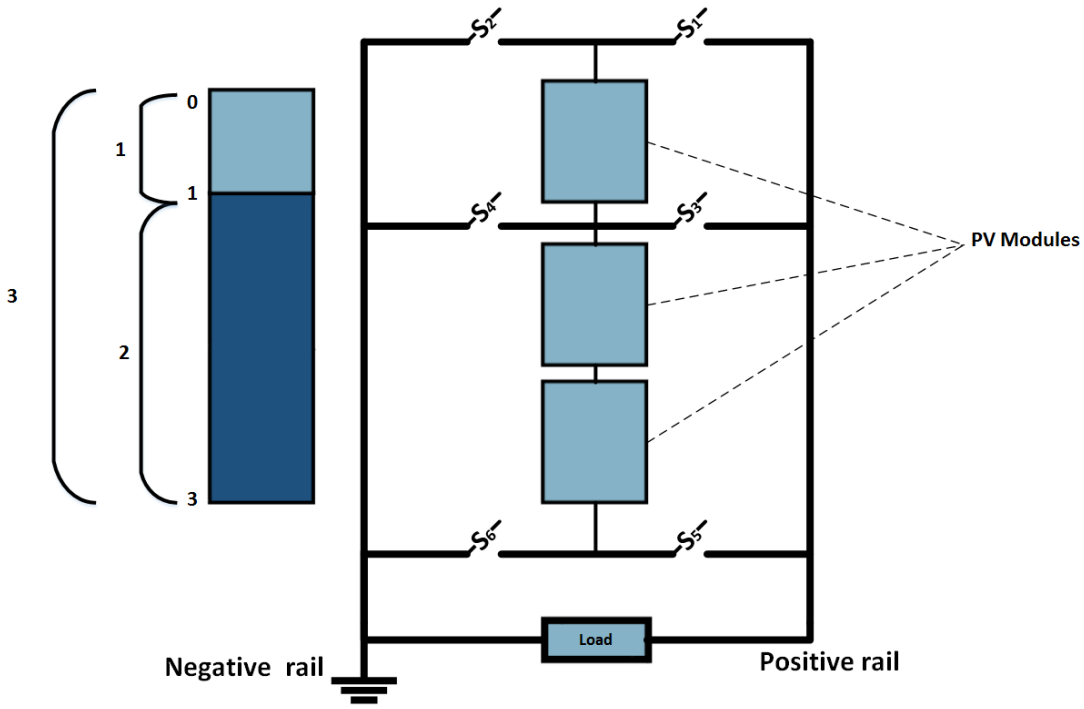

Figure 3.4: Basic structure of six-level Golomb inverter

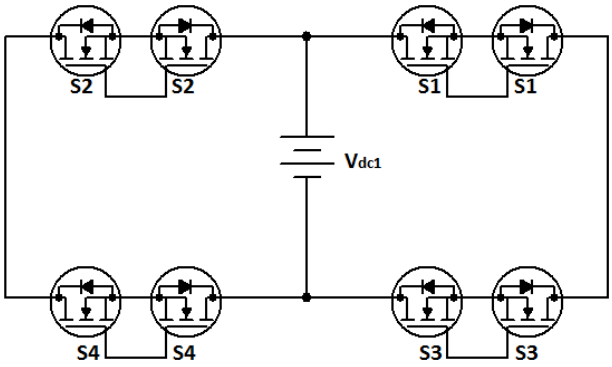

Figure 3.5: Configuration of one DC-source (V_{dc1}) within the Golomb inverter

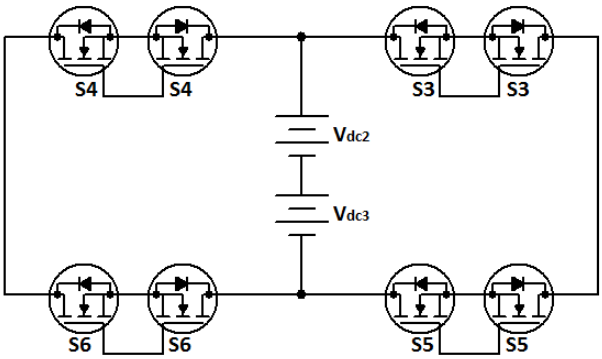

Figure 3.6: Configuration of two DC-sources (V_{dc2}, V_{dc3}) within the Golomb inverter

It is worth noting that both the number of switches (N_s) and the output levels (L) in full cycle (0 to 2π) without including zero level are directly related to the order of the ruler (n) as given in equation (3.23). However, the required number of DC sources (R) depends mainly on the length of the ruler (a_n) as illustrated in Table 3.6.

A straightforward generalization is expressed as follows:

$$L = (n-1)n \tag{3.22}$$

$$N_s = 2n \tag{3.23}$$

$$R = a_n \tag{3.24}$$

Table 3.6: The number of switches versus the number of output levels in Golomb topologies

Order n	Ruler	D	R	L	N_s
3	[0 1 3]	3	3	6	6
4	[0 1 4 6]	6	6	12	8
5	[0 1 4 9 11]	10	11	20	10
6	[0 1 4 10 12 17]	15	17	30	12
7	[0 1 4 10 18 23 25]	21	25	42	14
:	:	:	:	:	:
:	:	:	:	:	:
n	[a_1 a_2 a_3 ..... a_n]	x	a_n	$(n-1)n$	$2n$

Table 3.6 shows that both the number of the required MOSFET switches and output levels increase linearly with the order. In fact, the number of the output levels is exactly twice the number of increments (D) that can be measured by Golomb ruler as previously given by equation (3.3).

It can be concluded from Table 3.6 that the third-order Golomb structure saves two MOSFET switches compared to the switch ladder multilevel inverter proposed in [77]. The seven-level topology documented in [77] consists of eight MOSFET switches and three sources. Furthermore, the 6-level, Golomb topology saves 6 MOSFET switches compared to 7-levels conventional H-bridge inverter [78]. The latter consists of three DC sources and 12 switches.

3.4.2 Direct Switching Control Strategy

The control scheme applied to the proposed inverter here is based on a direct switching on and switching off strategy. This means that at any instant the controlled switching devices are either turned on or off at a low frequency to synthesize a near sinusoidal waveform.

There are six different switching states to generate the desired 6 - level output voltage waveform from the proposed inverter here. At all time instants in both positive or negative cycle, there are only two switches conducting (turned on). The output voltage levels of a full period 2π of the proposed inverter can be expressed as a linear combination of V_{dc1} and (V_{dc2}+ V_{dc3}) as in equation (3.25).

$$V_{out} = u_1 V_{dc1} + u_2(V_{dc2} + V_{dc3}) \qquad \forall \quad u_1, u_2 \in \{-1, 0, 1\} \tag{3.25}$$

The DC voltages (PV sources) of this inverter are fixed according to the third - order Golomb ruler [0 1 3] as given in (3.26).

$$V_{dc1} = \frac{V_{dc2} + V_{dc3}}{2} \tag{3.26}$$

There are seven valid states of (u_1,u_2) out of nine possible combinations in the linear expression shown in equation (3.25) which are (0,0),(1,0),(0,1),(-1,0),(0,-1),(1,1) and (-1,-1). However, the states (-1,1) and (1,-1) cause a short circuit at the terminals of the DC sources, and further the (0,0) state is not included in the control stage of the proposed inverter. Therefore, zero DC level is not produced in the output waveform. All the switching states of the proposed inverter are presented in Figures 3.7, 3.8,

3.9, 3.10, 3.11 and 3.12 with positive current paths. The load voltage is $+V_{dc1}$ with a positive current path as shown in Figure 3.7 while Figure 3.8 and Figure 3.9 present the output levels of $+(V_{dc2}+V_{dc3})$ and $+(V_{dc1}+V_{dc2}+V_{dc3})$ respectively with positive current paths. However, the output voltage levels in Figure 3.10, Figure 3.11 and Figure 3.12 are -V_{dc1}, -$(V_{dc2}+V_{dc3})$ and -$(V_{dc1}+V_{dc2}+V_{dc3})$ respectively with positive current paths.

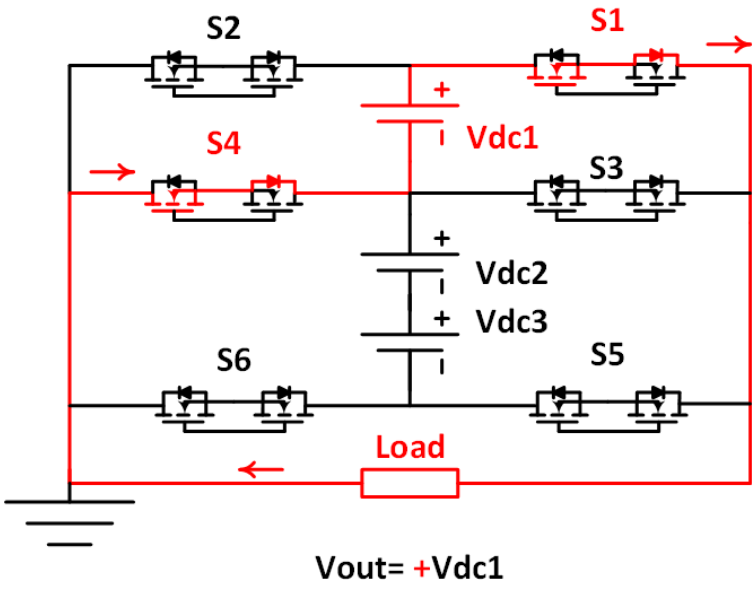

Figure 3.7: The current path for the proposed inverter when $V_{out} = +V_{dc1}$

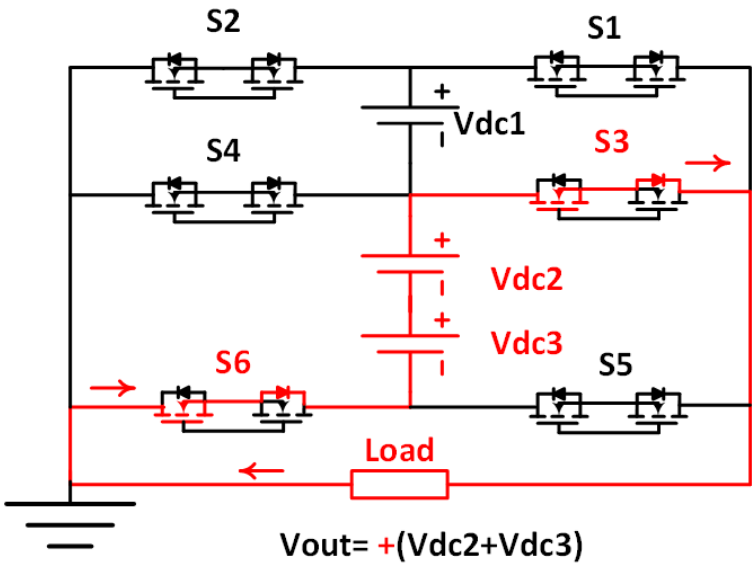

Figure 3.8: The current path for the proposed inverter when $V_{out} = +(V_{dc2} + V_{dc3})$

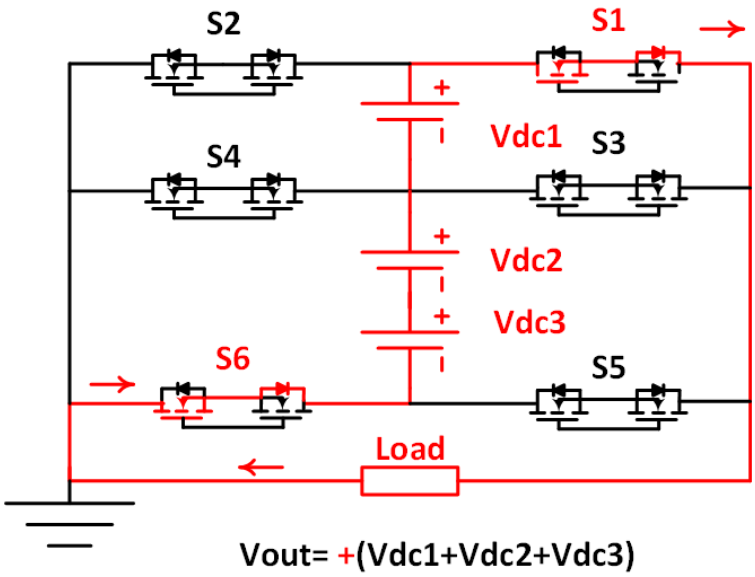

Figure 3.9: The current path for the proposed inverter when $V_{out} = +(V_{dc1}+V_{dc2}+V_{dc3})$

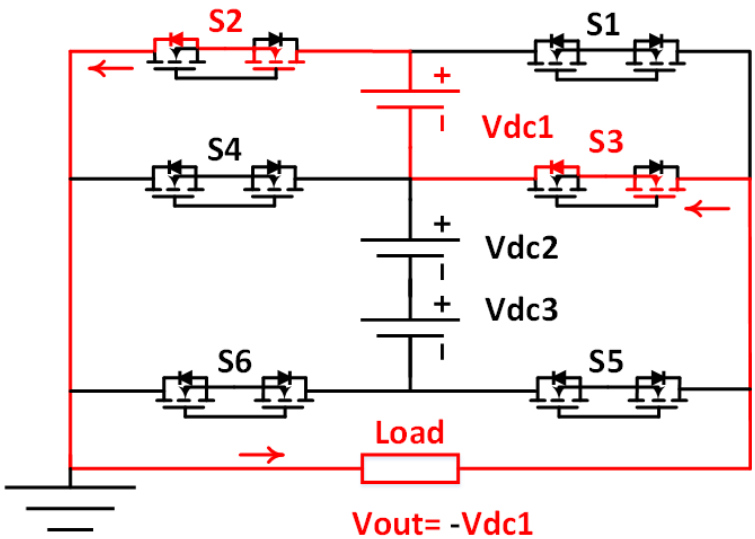

Figure 3.10: The current path for the proposed inverter when $V_{out} = -V_{dc1}$

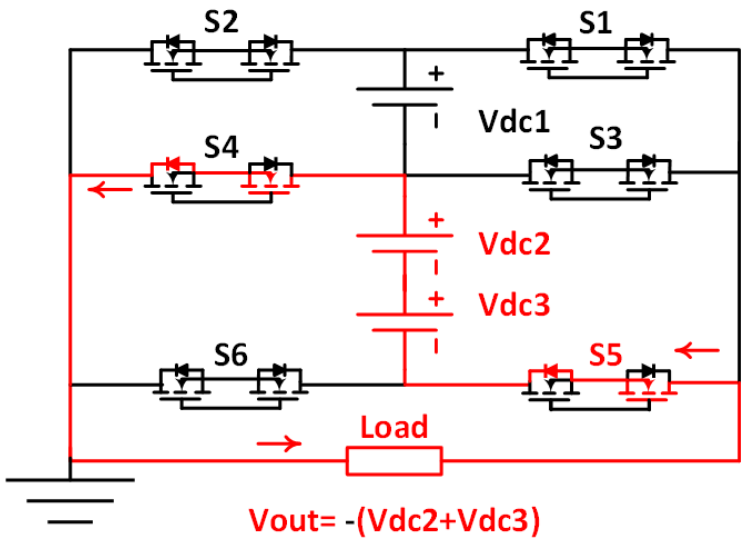

Figure 3.11: The current path for the proposed inverter when $V_{out} = -(V_{dc2} + V_{dc3})$

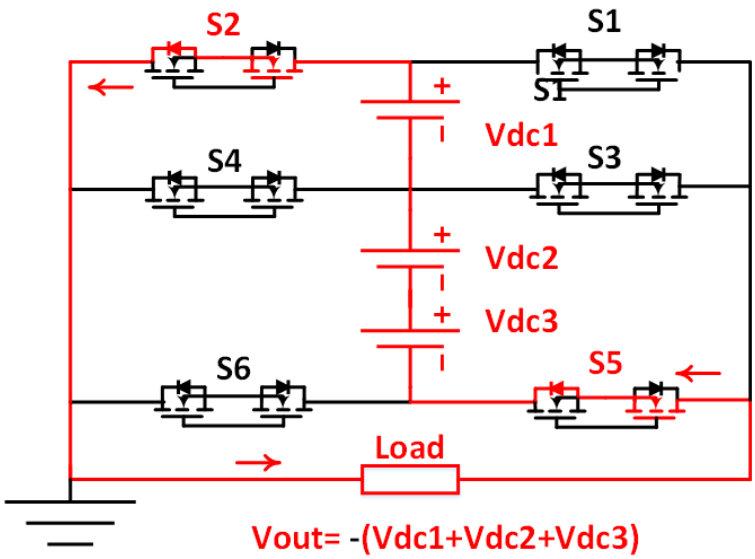

Figure 3.12: The current path for the proposed inverter when $V_{out} = -(V_{dc1} + V_{dc2} + V_{dc3})$

Table 3.7 and Table 3.8 demonstrate the switching strategy for 6 level Golomb inverter in positive and negative half cycles, respectively. Table 3.7 shows that if S_1 and S_4 are conducting while S_2, S_3, S_5 and S_6 are off, $+V_{dc1}$ is generated across the load terminals for T_1 time duration. If S_3 and S_6 are switched on, the output voltage equals to $+(V_{dc2} + V_{dc3})$ for T_2 time duration and so on. Table 3.8 illustrates that the output voltage is $-V_{dc1}$ if only S_2 and S_3 are conducting. If S_4 and S_5 are switched on, the output voltage equals to $-(V_{dc2} + V_{dc3})$ and so on. Clearly, Table 3.7 and Table 3.8 show the fact that at any instant only two switches are conducting and others are off.

Table 3.7: Switching states for six levels Golomb inverter of the positive half cycle

S_1	S_2	S_3	S_4	S_5	S_6	Output	duration
1	0	0	1	0	0	$+V_{dc1}$	T_1
0	0	1	0	0	1	$+(V_{dc2}+V_{dc3})$	T_2
1	0	0	0	0	1	$+(V_{dc1}+V_{dc2}+V_{dc3})$	T_3
1	0	0	0	0	1	$+(V_{dc1}+V_{dc2}+V_{dc3})$	T_3
0	0	1	0	0	1	$+(V_{dc2}+V_{dc3})$	T_2
1	0	0	1	0	0	$+V_{dc1}$	T_1

Table 3.8: Switching states for six levels Golomb inverter of the negative half cycle

S_1	S_2	S_3	S_4	S_5	S_6	Output	duration
0	1	1	0	0	0	$-V_{dc1}$	T_1
0	0	0	1	1	0	$-(V_{dc2}+V_{dc3})$	T_2
0	1	0	0	1	0	$-(V_{dc1}+V_{dc2}+V_{dc3})$	T_3
0	1	0	0	1	0	$-(V_{dc1}+V_{dc2}+V_{dc3})$	T_3
0	0	0	1	1	0	$-(V_{dc2}+V_{dc3})$	T_2
0	1	1	0	0	0	$-V_{dc1}$	T_1

It is also obvious from the Table 3.7 and Table 3.8 that each switch in the proposed inverter in this chapter is loaded equally in one complete cycle (four times/per cycle). For example, S_1 is conducting four times in one complete cycle 2π. S_1 conducts twice to generate $+V_{dc1}$ and further two times to generate $+(V_{dc1} + V_{dc2} + V_{dc3})$. Additionally, S_2 conducts twice to produce $-V_{dc1}$ and further two times to produce $-(V_{dc1}+V_{dc2}+V_{dc3})$. It can be deduced from the switching states tables that the output voltage signal has 12 segments in one complete cycle 0 to 2π as depicted in Figure 3.13. The timing duration of switching each level T_x (x = 1, 2 and 3) of a known amplitude 50 Hz multilevel signal is optimized using a completely new mathematical method which is discussed in detail in Chapter 5. However, a heuristic technique is used to determine the timing steps of the voltage output of the experimental Golomb

prototype (see section 3.6.1 for details).

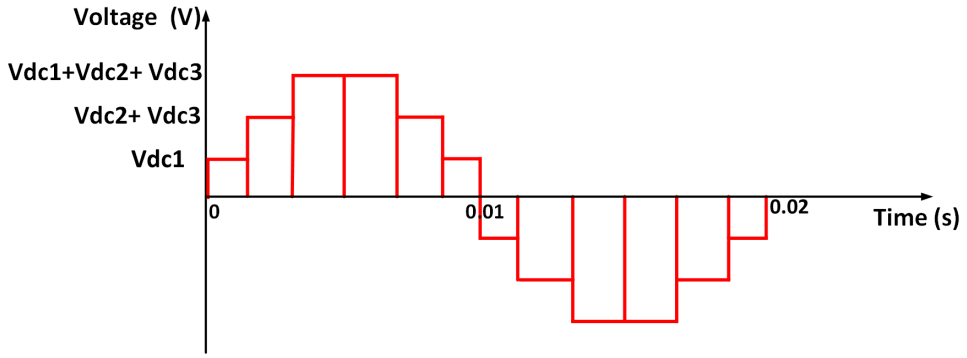

Figure 3.13: Segmented 6 - level voltage waveform (12 segments shown)

The overall switching frequency f_{sw} of the proposed inverter is determined approximately by the number of segments in one complete cycle as given in equation (3.27).

$$f_{sw} = S_g.f_{fundamental} \tag{3.27}$$

where $f_{fundamental}$ is the fundamental frequency (50 Hz), and S_g is the number of segments in the output signal in one complete cycle 0 to 2π.

3.5 Performance of Golomb Inverter

3.5.1 Golomb Inverter Power Switching Losses

In general, waveforms generated by practical inverters contain harmonic contents and are non - sinusoidal. Harmonic components at the output of the DC-to-AC inverter can be eliminated by applying PWM techniques or using a filter circuit. The latter

approach has a drawback of a large size and cost. PWM techniques however reduce the filter requirements to a minimum at the expense of higher switching losses, production of common mode voltages and a large switching stress [79]. Multilevel inverters are desirable for renewable energy systems, precisely those related to photovoltaic applications. In fact, multilevel inverters overcome the issues of the conventional PWM inverters by offering the advantages of a less switching stress at high voltages, switching at low frequency and hence minimizing both harmonic contents and power switching losses.

In order to determine the switching losses of the Golomb inverter shown in Figure 3.4, the power lost through each MOSFET due to switching while conducting is mathematically determined in this section. The losses through a MOSFET switch are mainly caused by the following facts:

1. The on state voltage drop across the MOSFET switch is non - zero $V_{dc} \neq 0V$, V_{dc} (known as saturation voltage). This causes a conduction loss that can be calculated as the product of the device current and the forward saturation voltage [80].

2. The off state current through the MOSFET leakage current is non - zero $I_{leakage} \neq 0A$. This causes a blocking loss which can be calculated in a straightforward manner as the product of the blocking voltage and the leakage current [79].

3. Transition time (on-to-off states) $t_{off} \neq 0$ and (off-to-on states) $t_{on} \neq 0$

Consider a case of a single MOSFET switch connected across a DC voltage source of a maximum value of V_{max} through a resistive load as shown in Figure 3.14. The

current through the MOSFET switch is considered as I_{max} during the on state while it is 0 A during the off state. The voltage is maximum (V_{max}) during the off state while it is 0 V during the on state as clearly illustrated in Figure 3.15.

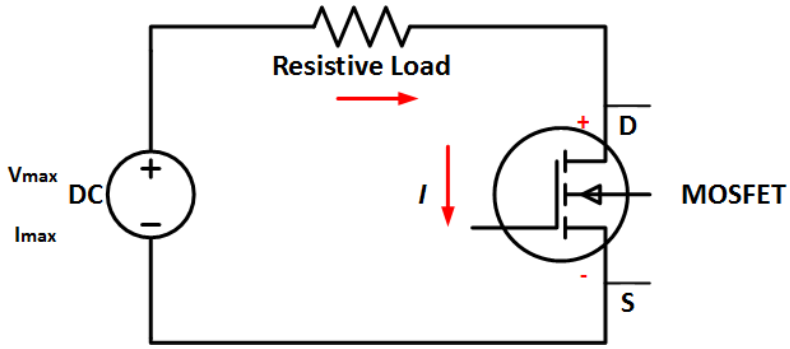

Figure 3.14: Circuit diagram of a single MOSFET connected to a DC source

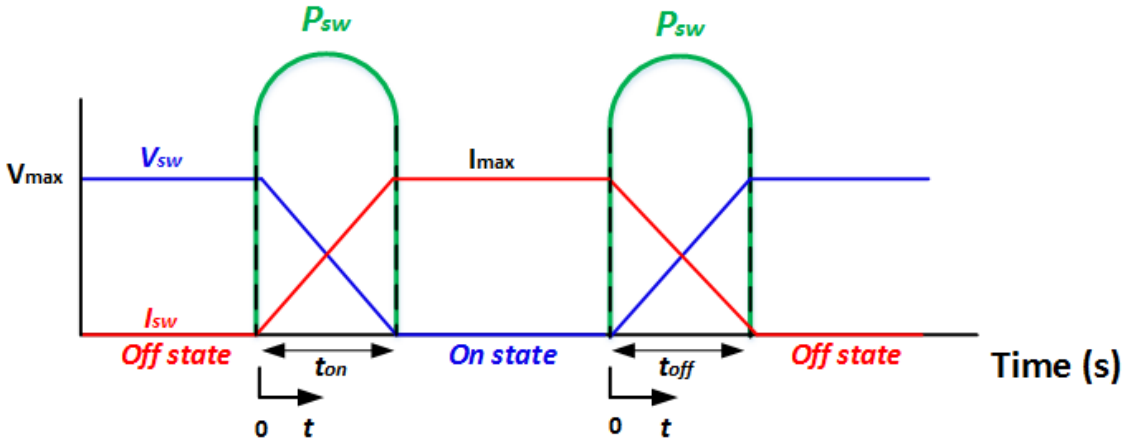

Figure 3.15: Linearized switching characteristics

Switching losses can be calculated from turn - on and turn - off states of the MOSFET. Instantaneous voltage and current during turn - on time t_{on} can be extracted from Figure 3.15 as in equation (3.28) and equation (3.29) respectively. Figure 3.15 has shown clearly that the voltage during turn - on transition t_{on} falls from V_{max} to zero

and the current rises from zero to I_{max}.

$$V_{sw}(t) = V_{max}(1 - \frac{t}{t_{on}}) \tag{3.28}$$

$$I_{sw}(t) = I_{max}\frac{t}{t_{on}} \tag{3.29}$$

The instantaneous power switching losses through a single MOSFET switch during t_{on} interval can be written as equation (3.30).

$$\begin{aligned} P_{sw}(t) &= V_{sw}(t).I_{sw}(t) \\ &= (V_{max}.I_{max})\frac{t}{t_{on}}(1 - \frac{t}{t_{on}}) \end{aligned} \tag{3.30}$$

The energy dissipated during this interval t_{on} is given by equation (3.31).

$$\begin{aligned} E &= \int_0^{t_{on}} P_{sw}(t)dt \\ &= \int_0^{t_{on}} V_{sw}(t).I_{sw}(t)dt \\ &= \int_0^{t_{on}} ((V_{max}.I_{max})\frac{t}{t_{on}}(1 - \frac{t}{t_{on}}))dt \\ &= V_{max}.I_{max}\int_0^{t_{on}} \frac{t}{t_{on}}(1 - \frac{t}{t_{on}})dt \\ &= \frac{V_{max}.I_{max}.t_{on}}{6} \end{aligned} \tag{3.31}$$

Hence, the average switching loss in the switch during the transition of turn - on can be obtained by equation (3.32).

$$P_{sw} \downarrow_{t_{on}} = \frac{V_{max}.I_{max}.t_{on}.f_{sw}}{6} \tag{3.32}$$

where f_{sw} is the switching frequency.

The instantaneous voltage and current during turn - off transition t_{off} can be expressed as equation (3.33) and equation (3.34) respectively.

$$V_{sw}(t) = V_{max}\frac{t}{t_{off}} \tag{3.33}$$

$$I_{sw}(t) = I_{max}(1 - \frac{t}{t_{off}}) \tag{3.34}$$

The instantaneous power switching losses through a single MOSFET switch during t_{off} interval can be written as equation (3.35).

$$\begin{aligned} P_{sw}(t) &= V_{sw}(t).I_{sw}(t) \\ &= (V_{max}.I_{max})\frac{t}{t_{off}}(1 - \frac{t}{t_{off}}) \end{aligned} \tag{3.35}$$

Integrating the instantaneous power during the turn off time over the range of (0 to t_{off}), results in the energy dissipated during t_{off} interval as given in equation (3.36).

$$\begin{aligned} E &= \int_0^{t_{on}} P_{sw}(t)dt \\ &= \frac{V_{max}.I_{max}.t_{off}}{6} \end{aligned} \tag{3.36}$$

With the switching frequency of f_{sw}, the average switching power loss in a single MOSFET switch during the transition of turn off time can be written as equation (3.37).

$$P_{sw}\downarrow_{t_{off}} = \frac{V_{max}.I_{max}.t_{off}.f_{sw}}{6} \tag{3.37}$$

Hence, the overall average switching loss P_{sw} in a single switch is shown in equation

(3.38).

$$\begin{aligned} P_{sw}\downarrow_{Total} &= P_{sw}\downarrow_{t_{on}} + P_{sw}\downarrow_{t_{off}} \\ &= \frac{V_{max}.I_{max}.t_{on}.f_{sw}}{6} + \frac{V_{max}.I_{max}.t_{off}.f_{sw}}{6} \\ &= \frac{V_{max}.I_{max}.f_{sw}}{6}(t_{on} + t_{off}) \end{aligned} \tag{3.38}$$

Assuming $t_{on} = t_{off} = t_{tran}$ in equation (3.38), results in a simplified equation (3.39).

$$\begin{aligned} P_{sw}\downarrow_{Total} &= \frac{2.V_{max}.I_{max}.f_{sw}.t_{tran}}{6} \\ &= \frac{V_{max}.I_{max}.f_{sw}.t_{tran}}{3} \end{aligned} \tag{3.39}$$

Equation (3.39) shows that the switching power loss in MOSFET switches varies linearly with the switching frequency and the switching transition times.

In section 3.4.2, we showed that there are only two switches conducting in the Golomb ruler at each particular instant and hence the overall switching losses in Golomb inverter is written as in equation (3.40). The voltage in the relationship is the maximum supply voltage that MOSFET will experience. The overall switching of Golomb topology is given in equation (3.40) as there is only two MOSFET switches conducting at each instant.

$$P_{sw}\downarrow_{Inverter} = \frac{2.V_{max}.I_{max}.f_{sw}.t_{tran}}{3} \tag{3.40}$$

With regards to the switching losses during transition time (on to off and off to on states), equation (3.40) illustrates clearly the fact that the Golomb inverter with 6 MOSFET switches is equivalent to a circuit with two MOSFET switches.

Taking a panel of maximum voltage of 33.7 V at $I_{max} = 3.56$ A [81], and assuming

t_{tran} = 100 ns, the overall switching losses by Golomb switch PV panel $P_{sw} \downarrow_{Golomb}$ are compared to high frequency switching $f_{sw} \downarrow_{PWM}$= 100 kHz (PWM) control method at different installation voltages and number of levels L (without zero incorporated as previously presented in Table 3.6). The number of levels will change the switching frequencies $f_{sw} \downarrow_{Golomb}$ of the Golomb structure. The Golomb switching frequency is identified by using the uniform sampling method previously presented in section 3.4.2. Table 3.9 summarizes the switching losses of the high frequency PWM control method and the Golomb switch structure (based on third, fourth and fifth order Golomb rulers).

Table 3.9: Golomb switching losses versus PWM switching losses at different number of levels and installation voltages

L	Installation (V)	$P_{sw} \downarrow_{PWM}$	$f_{sw} \downarrow_{Golomb}$	$P_{sw} \downarrow_{Golomb}$
6	101.1	2.4 W	600 Hz	14.3 mW
12	202.2	4.8 W	1.2 kHz	57.5 mW
20	370.7	8.8 W	2 kHz	157.9 mW

It is clear from Table 3.9 that using the Golomb switch panel would reduce $P_{sw} \downarrow_{PWM}$= $2.4W$ loss to only 14.3 mW, $P_{sw} \downarrow_{PWM}$= $4.8W$ to 57.7 mW and $P_{sw} \downarrow_{PWM}$= $8.8W$ to 157.9 mW due to the fact that the Golomb switch control runs at the order of 1000 times lower frequency than a conventional PWM control method.

The performance of both the PWM control method and the Golomb switch structure at various installation voltages is depicted in Figure 3.16. This figure clearly indicates that the switching losses in the Golomb structure are lower than that of the PWM control method by an order of 167, 83, and 50 at installation of 101.1 V, 202.2 V and 370.7 V respectively.

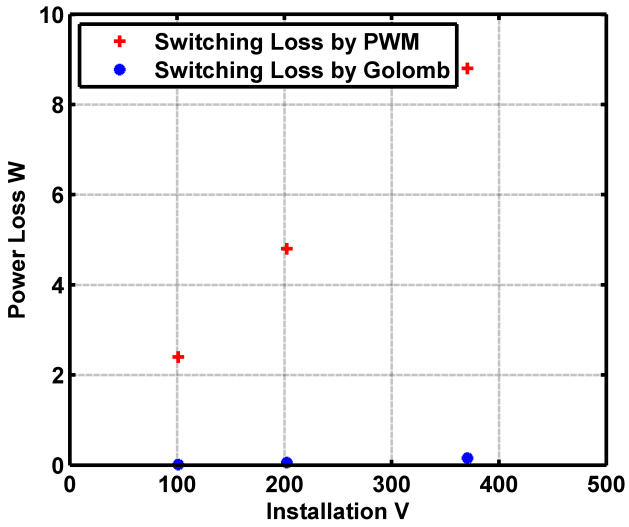

Figure 3.16: Golomb switching loss versus PWM switching loss at different installation voltages

3.5.2 PV Panel Series Resistance-Based Dissipation

The ideal solar cell is equivalent to a current generator connected in parallel with a diode (non-linear resistive element). In fact, the real solar cells are not perfect due to the appearance of the contact and leakage current resistances which are known as series and shunt resistance, respectively. The power is dissipated through leakage current and through the resistance of the contacts around the sides of the device [82]. The internal series resistance arises from the resistance of the cell material to current flow through the front surface to the contacts in particular [82]. In fact, the internal series resistance of a PV panel is one of the important parameters which characterizes its health and describes both internal losses and losses due to poor contacts [81], [83]. Particularly, series resistance is a problem at high irradiation levels and this further causes high current densities [82].

In the Golomb inverter, the selection of a minimum PV cell count to produce a close approximation to a sine-wave voltage means the effective total series resistance of the PV panels is modulated by the output voltage. Therefore, the average resistance is given by equation (3.41).

$$R_{av} = \frac{R_{series}}{\pi} \int_0^{\pi} \sin(\theta) d\theta = \frac{2R_{series}}{\pi} \tag{3.41}$$

where R_{series} is the PV panel series resistance. This is a 36% reduction in the series resistance power dissipation over the conventional contiguous block arrangement. In fact, the average resistance in the normal contiguous block arrangement is equal to the series resistance and this is 100% dissipation. Equation (3.41) shows 63% dissipation which is 36% less series resistance loss compared to the conventional block arrangement. This means that the power loss due to the PV series resistance in the Golomb inverter can be written as:

$$P_{loss} = \alpha_{loss}.R_{series}.I_{max}^2 \tag{3.42}$$

where α_{loss} is the loss reduction factor ($\alpha_{loss} = 0.36$), and I_{max} is the PV maximum current.

For instance, taking R_{series} as 2 ohm for a 33.7 V panel at $I_{max} = 3.56$ A [81], the power loss P_{loss} at different installation voltages is tabulated in Table 3.10.

Table 3.10: Power saving of Golomb topology with R_{series}

Installation	R_{series}	Power saving$\downarrow_{Golomb}$
101 V	6 Ω	27.25 W
202 V	12 Ω	54 W
404 V	24 Ω	109 W
480 V	28 Ω	127 W
520 V	30 Ω	136.8 W

It is shown in Table 3.10 that the Golomb inverter gives a power saving of 54 W in the case of 202 V installation and twice that value at 404 V installation.

3.5.3 Overall Utilization of PV Panel in the Third - order Golomb Inverter

There are only three PV sources employed in the third - order Golomb inverter as previously mentioned in section 3.4.1. In fact, the PV sources in Golomb inverter are unevenly utilized as explained in the control section 3.4.2. In this work, we show the percentages of utilizing each PV source in Golomb inverter (third - order configuration) in a quarter - cycle analysis. Assuming that A, B and C are the PV sources that perform the third - order Golomb configuration as in Figure 3.17. The steps of the output signal in a quarter - cycle are generated by the switching technique explained in section 3.4.2 and illustrated in Figure 3.18.

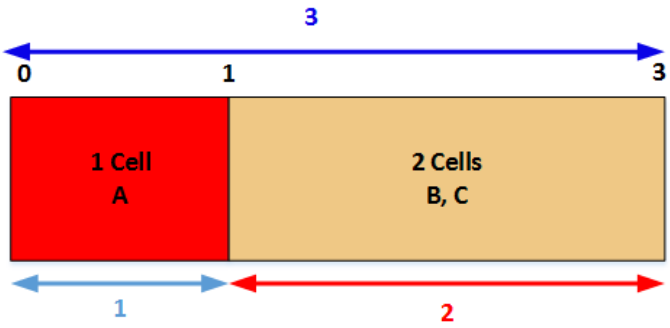

Figure 3.17: Third-order Golomb Ruler

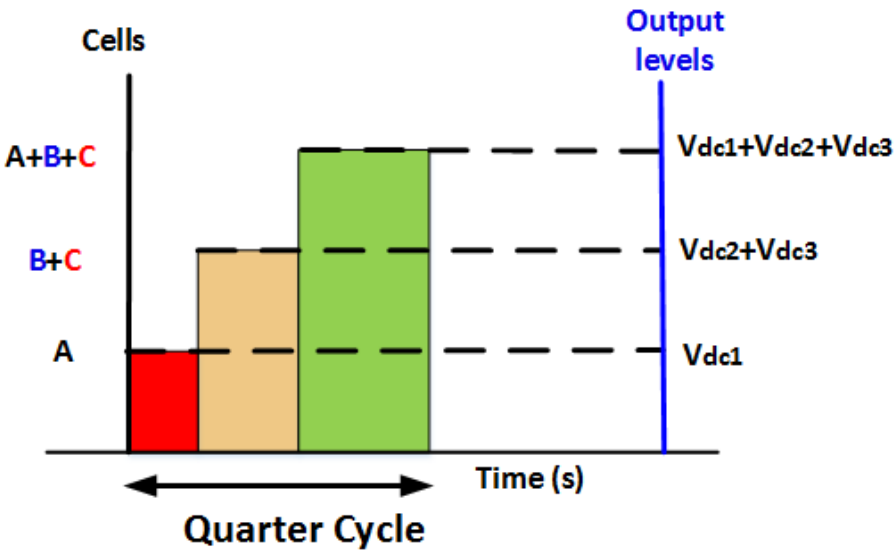

Figure 3.18: Three-level output signal in a positive quarter cycle showing the cells and their contribution to the output levels

It is seen from Figure 3.18 that the positive quarter cycle that cell A is utilized twice to generate the following voltage steps of $+V_{dc1}$ and $+(V_{dc1}+V_{dc2}+V_{dc3})$. This clearly indicates a total average of two - thirds (66.66%) of cell A utilization in a quarter cycle. Additionally, cell B is utilized twice over the quarter positive cycle which means a total average of 66.66% cell utilization. Cell B performs the voltage levels

of $+(V_{dc2} + V_{dc3})$ and $+(V_{dc1} + V_{dc2} + V_{dc3})$. Cell C is utilized twice in the quarter cycle to perform the voltage levels of $+(V_{dc2} + V_{dc3})$ and $+(V_{dc1} + V_{dc2} + V_{dc3})$. This is also two - thirds of a total cell C utilization. Although the percentage of utilizing the cells are equal but this does not indicate that the cells are used evenly at each output level. Table 3.11 illustrates the number of instants at which each individual PV cell (A, B and C) is utilized in the positive quarter cycle.

Table 3.11: The number of utilization instances of each PV panel in the positive quarter cycle

Output Voltage Level	PV Cells		
	A	B	C
$+V_{dc1}$	1	0	0
$+(V_{dc2} + V_{dc3})$	0	1	1
$+(V_{dc1} + V_{dc2} + V_{dc3})$	2	2	2

Cell A is utilized twice in the quarter cycle to produce the voltage output levels of $+V_{dc1}$ (first usage 1) and $+(V_{dc1} + V_{dc2} + V_{dc3})$ (second usage 2) as illustrated clearly in Table 3.11. However, cell A is not utilized (not used 0) when the voltage output level of $V_{dc2} + V_{dc3}$ is generated. Further, cells B and C are utilized twice to generate the voltage levels of $+(V_{dc2} + V_{dc3})$ (first usage 1) and $+(V_{dc1} + V_{dc2} + V_{dc3})$ (second usage 2) while they are not utilized when voltage level ($+V_{dc1}$ is generated (not used 0). Table 3.11 shows clearly the redundancy (0) in the DC cells when the three levels in the positive quarter cycle are generated. Despite the fact that the cells are not fully utilized in the Golomb inverter, this design has significantly reduced the number of semiconductor switches by 50% compared to the conventional 7-Level (with zero level incorporated) H-bridge inverter with the same number of DC sources [84]. The question is, should multilevel inverters for PV applications be designed in terms of maximum efficiency or in terms of least complexity? Various attempts have been

made to reduce the circuit complexity of PV multilevel inverter. Jaydeep et al [58] proposed a single phase 7-level with a zero level incorporated multilevel inverter for PV systems which includes an H-bridge stage with level modular topology. The latter minimized the number of required semiconductor switches at the expense of PV sources redundancy.

In this work, a solution is made to overcome the redundancy and circuit complexity with cyclic selection configurations which will be discussed in next chapter.

3.6 Experimental Implementation

3.6.1 Third - Order Golomb Inverter Overall Layout

The laboratory implementation layout for the single-phase third order Golomb inverter is shown below in Figure 3.19. The major components of the setup are three PV sources (RVFM - G100 solar cell module - 0.45 V,100 mA) and six G3VM-351 A/D MOSFET relays (Logic level MOSFET). A 24 V (150 W) halogen capsule lamp is used as a illumination source. This is placed at an optimum distance from the PV cells (2 cm). Mbed NXP LPC1768 microcontroller is used in this work to control the MOSFET relays through six DigitalOut pins (Pin_{15}, Pin_{16}, Pin_{17}, Pin_{18}, Pin_{19} and Pin_{20}) via an on - line C++ compiler. The Mbed microcontroller is powered through a USB cable using a PC. The major components in this setup, PV module, MOSFET relays and Mbed microcontroller are mounted on a printed circuit board (PCB).

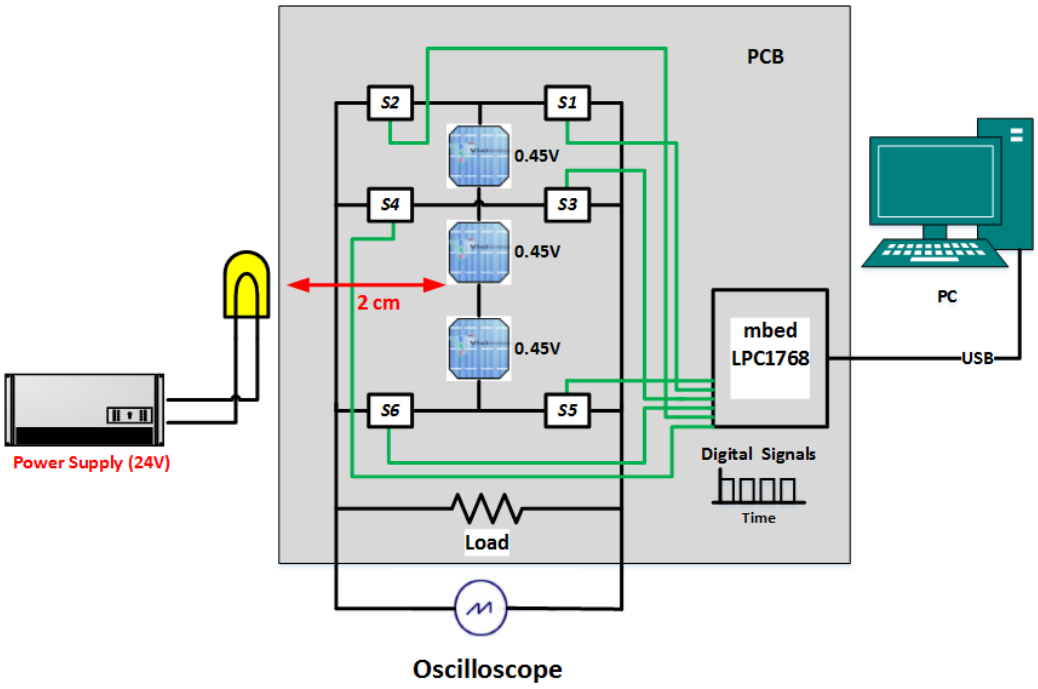

Figure 3.19: Implementation layout of the third-order Golomb inverter

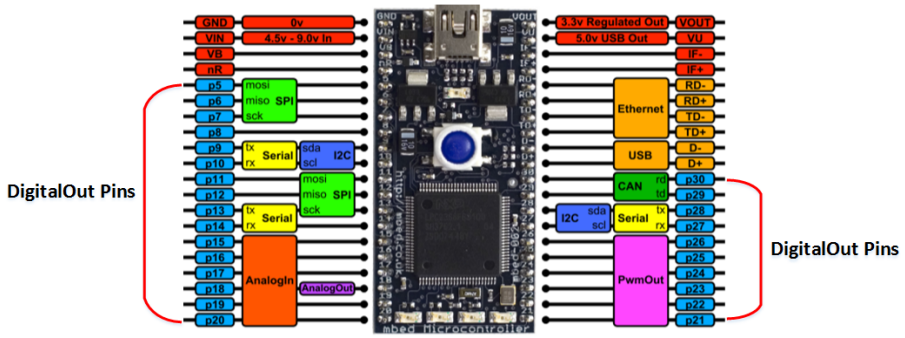

Figure 3.20: Picture of NXP LPC1768 MCU (ARM Cortex^{TM}-M3 Core) Mbed microcontroller module

Figure 3.20 shows the NXP LPC1768 MCU (ARM Cortex^{TM}-M3 Core) microcontroller module. It has 26 digital output pins that are set to high or low as required. The pins are marked with a red outline. Here, the microcontroller sets the states of the MOSFET relays according to the switching control scheme explained in section 3.4.2 to synthesize the required multilevel waveform. At any instant, each individual DigitalOut pin (Pin_{15} to Pin_{20}) is set either to zero to turn it off, or to 1 to turn it on to form the switching control signals for a full period 2π. Each digital signal goes to Pin_1 of each MOSFET relay to turn it on or turn it off. For example, the signal generated at Pin_{15} goes to S_1 to turn it on or off according to the switching scheme. To reach a high quality near sinusoidal 50 Hz output waveform, the time duration T_x (x=1,2 and 3) is determined by a sufficient heuristic technique used here for implementation purposes. This is based on a graphical approach to find the time coordinates of a fixed amplitude signal on a pure 50 Hz sinusoidal waveform of $+(V_{dc1} + V_{dc2} + V_{dc3})$ amplitude as shown in Figure 3.21.

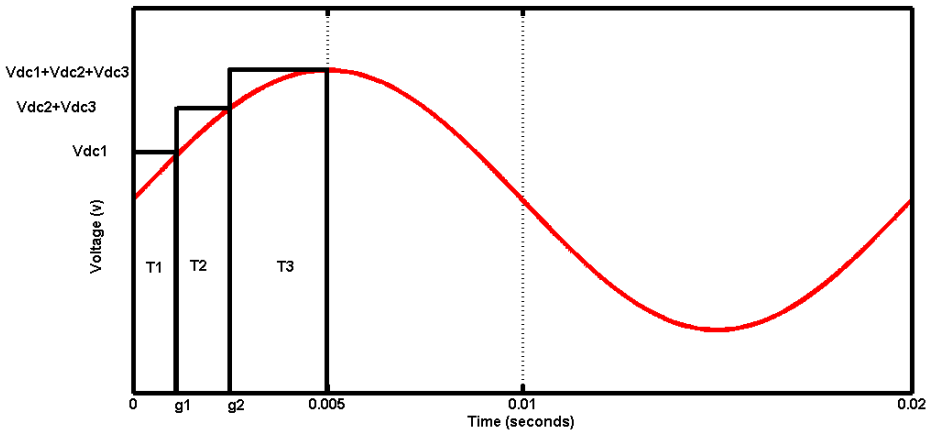

Figure 3.21: A heuristic technique for determining the timing steps of the 6-level Golomb inverter

Figure 3.21 shows just the first $\frac{\pi}{2}$ (0.005 s) segment as the $\frac{\pi}{2}$ (0.005 s) to π (0.01 s)

segment is a mirror image and the π (0.01 s) to 2π (0.02 s) region is a simple inversion. The initial step in determining the time coordinates for the positive quarter-cycle is to draw a line of each fixed amplitude V_{dc1}, (V_{dc2}+V_{dc3}) and (V_{dc1}+V_{dc2}+V_{dc3}) on the pure 50 Hz sinusoidal waveform and then using line dropping to find the time coordinates T_1,T_2 and T_3. The first line starts at point (0, V_{dc1}) and ends at the intersection point (g_1, V_{dc1}) to represent V_{dc1} level. The second line starts at point (g_1,V_{dc2}+V_{dc3}) and ends at the intersection point (g_2, V_{dc2}+V_{dc3}) to illustrate (V_{dc2}+V_{dc3}) level. The third line starts at point (g_2,V_{dc1}+V_{dc2}+V_{dc3}) and ends at the intersection point (0.005, V_{dc1}+ V_{dc2}+V_{dc3}) to present the (V_{dc1}+V_{dc2}+V_{dc3}) level. We found that the timing steps are ($T_1 = g_1$), ($T_2 = g_2 - g_1$) and ($T_3 = 0.005 - g_2$) in seconds such that ($T_1 = 0.0015$ s, $T_2 = 0.0017$ s, $T_3 = 0.0018$ s). The time steps in the implementation stage are further empirically adjusted to produce a good quality output. This technique can be only sufficient for a small number of levels. This can not guarantee a low total harmonic distortion THD. The time steps approximation of each individual control signal is set in the main program. The desired output multilevel waveform is captured at the load terminals through a oscilloscope. The switching control scheme is automated in C++ code (Appendix A). The overall pin configuration of the proposed inverter is shown in Figure 3.22.

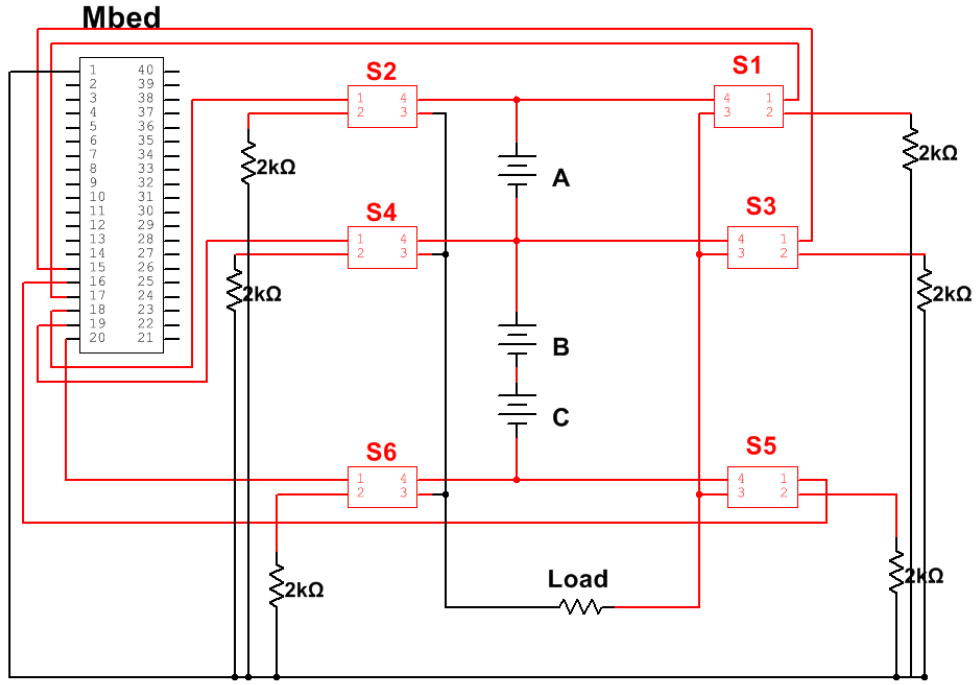

Figure 3.22: The circuit design of the third-order Golomb inverter

The internal circuit of the MOSFET relays includes an LED element which appears across Pin_1 and Pin_2 while two back to back MOSFETs appears across Pin_3 and Pin_4. Pin_1 of S_1,S_2,S_3,S_4,S_5, and S_6 is connected to the digital out pins of the Mbed Pin_{17}, Pin_{18}, Pin_{15}, Pin_{19}, Pin_{16} and Pin_{20} respectively. Pin_2 of each switch is connected to a limiting current resistance of 2 kΩ value to prevent the internal LED from burning up and then grounded in the Mbed side. Pin_3 of S_1, S_3 and S_5 are connected to a resistive load at the positive terminal of the inverter while Pin_3 of S_2, S_4 and S_6 are connected to the negative terminal. Pin_4 of both S_2 and S_1 is connected to the positive side of the PV module (A). The negative side of (A) is connected in series with the PV module (B) through the positive end and then to Pin_4 of both S_4 and

S_3. The negative side of (B) is connected to the positive side of the PV module (C). The negative end of (C) is connected to Pin_4 of both S_5 and S_6.

3.6.2 Component Characteristics

3.6.2.1 Solar Cell (RVFM - G100 Module)

Three solar cell modules are used to realized the third-order Golomb ruler (A, B, and C). The current-voltage (I - V) and power-resistance (P - R) characteristic curves of each cell are investigated by practical measurements as shown in Figure 3.23 and Figure 3.24 respectively.

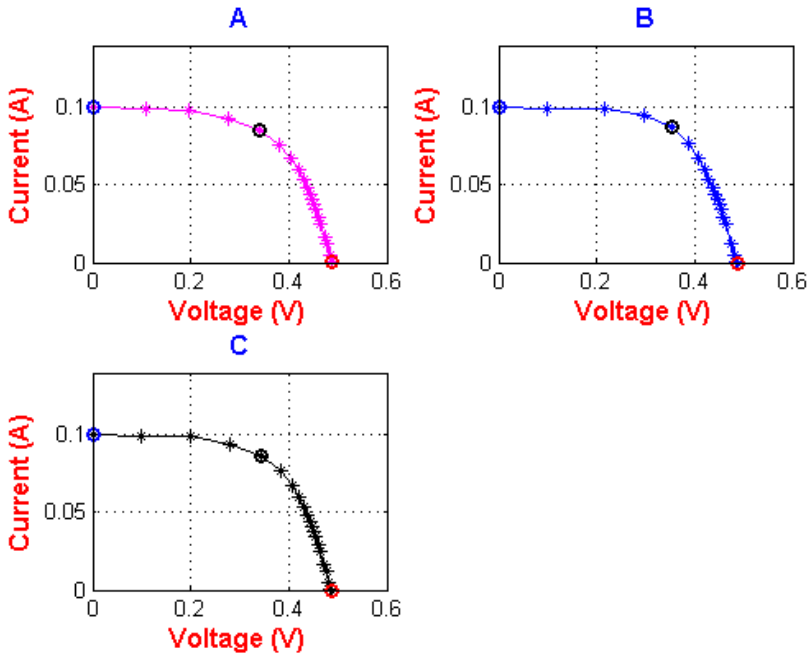

Figure 3.23: The experimental I-V characteristics of individual solar cell module at 100% light level

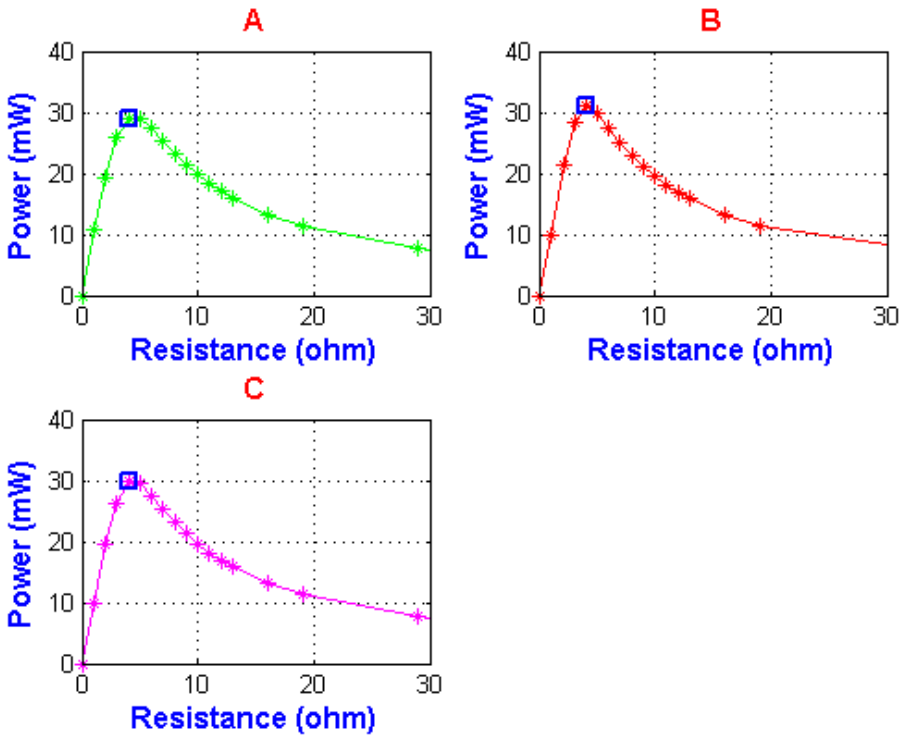

Figure 3.24: The experimental P-R characteristics of individual solar cell module at 100% light level

The greatest current produced by the cell is obtained under the short circuit conditions when the voltage vanishes, V = 0, and this current is called the short circuit current I_{sc} as outlined with a blue mark in the I - V curves. If the solar cell device is open circuit, it biases itself with a voltage that is called an open circuit voltage V_{oc} which is equal to the greatest voltage value when the current vanishes as shown clearly in the I - V curves (indicated with a red circle). The open circuit voltage and the short circuit current of each cell module extracted from the curves here are approximately 0.48 V and 100 mA respectively which are in very good agreement with the manufacturer specifications. The maximum power point (V_{MPP}, I_{MPP}) is indicated with a black mark in the I - V curve while with a blue mark in the P - R

curves (R_{opt}, P_{MPP}). The maximum power that each module can produce is approximately 30 mW at 4 Ohm optimum load. The series combinations of the two cells (B and C), and three cells (A, B and C) are also tested at 100% light levels as shown in Figure 3.25. It is very clear from Figure 3.25 and Figure 3.23 that V_{oc} of B+C is higher than the individual V_{oc} of B and C. Yet, I_{sc} is approximately equal in the series combination of (B+C) and individual B and C.

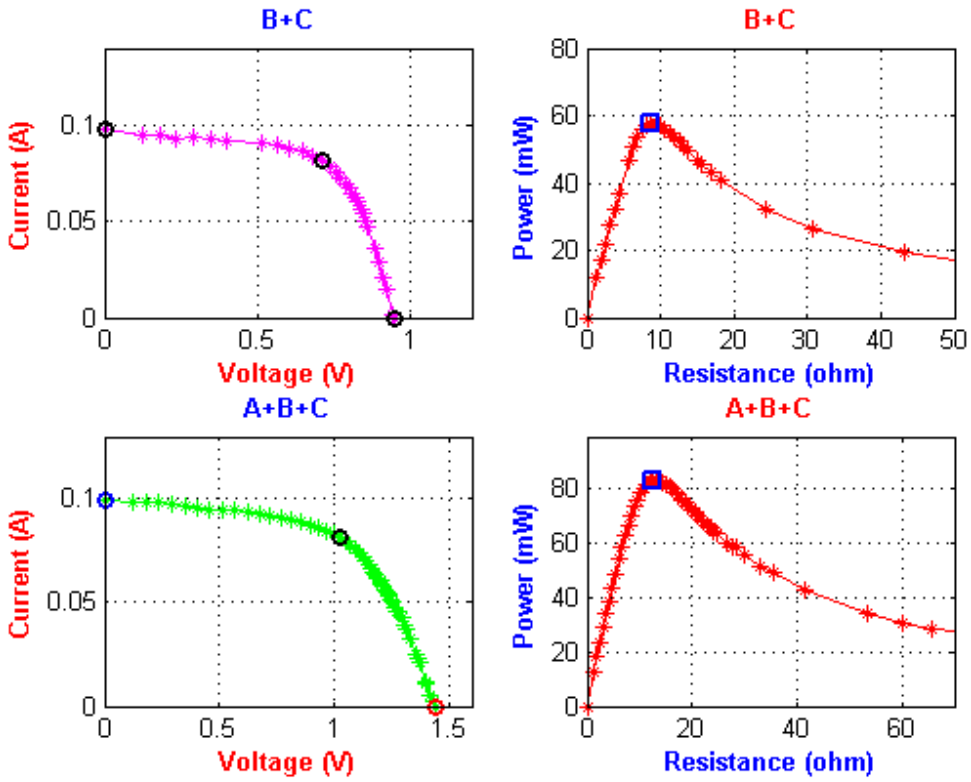

Figure 3.25: The experimental (I-V) and (P-R) characteristics of two and three series solar cell modules at 100% light level

Table 3.12 summarizes the electrical performance of the individual cells and their series combinations.

Table 3.12: The electrical performance of the individual PV modules and their series combinations

Electrical Performance	PV Cells				
	A	B	C	B+C	A+B+C
I_{sc}	100 mA	100 mA	100 mA	99.8 mA	99.6 mA
V_{oc}	0.48 V	0.48 V	0.47 V	0.94 V	1.444 V
V_{MPP}	0.3410 V	0.35 V	0.3450 V	0.7110 V	1.0250 V
I_{MPP}	86.5 mA	86.0 mA	86.2 mA	81.3 mA	81.0 mA
P_{MPP}	29.5 mW	30.1 mW	29.7 mW	57.8 mW	83 mW
R_{opt}	4 ohm	4.1 ohm	4 ohm	8.75 ohm	12.65 ohm

It can be deduced from Table 3.12 that the characteristics of the series combinations of (B+C) and (A+B+C) are in a very good agreement with the individual characteristics. For example, the optimum load resistance of (B+C) and is approximately twice (8.75 ohm) the individual optimum loads of B and C while it is roughly triple (12.56 ohm) the individual loads in the case of (A+B+C).

3.6.2.2 G3VM-351 A/D MOSFET Relays

The PV sources are directly switched using 6 MOSFET relays as previously detailed. These switching modules have optical isolation between the field side and control side with 4 pins (Pin_1, Pin_2,Pin_3 and Pin_4). The internal LED of the relay is turned on when the control signal is 3.3 V that is generated from the DigitalOut pin of the microcontroller and thus the internal back to back MOSFET is switched on. The switching capability of the relays are investigated by a switching low voltage PV module across the output pins of the relay. This initial step is carried out to ensure that the relays can switch low voltage PV modules of 0.45 V, 0.9 V and 1.4 V which presents the output levels of the proposed inverter. Figures 3.26, 3.27 and 3.28 show

the capabilities of the relays at 0.45 V, 0.9 V and 1.4 V respectively.

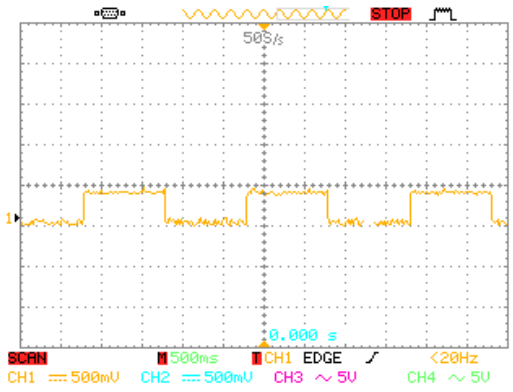

Figure 3.26: The switching capability of the relays at 0.45 V level

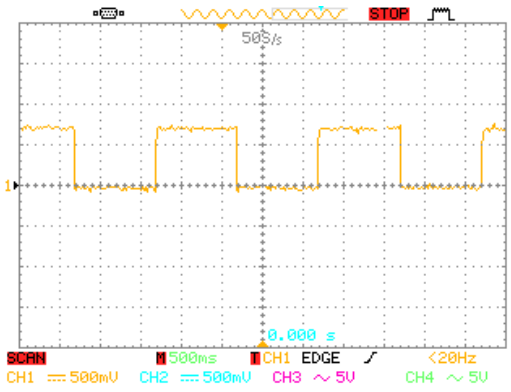

Figure 3.27: The switching capability of the relays at 0.9 V level

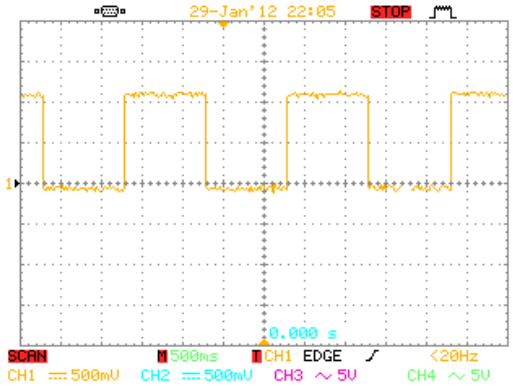

Figure 3.28: The switching capability of the relays at 1.4 V level

It can be concluded from the figures 3.26, 3.27 and 3.28 that the relays are capable of switching low voltage levels with a good accuracy.

3.7 Experimental and Simulation Results

3.7.1 Third-order, DC-to-AC Golomb Multilevel inverter Simulation

The Simulink simulation of the single-phase, 6-level, 50 Hz DC-to-AC, Golomb inverter requires a switching controller block that can control each MOSFET switch according to the switching states previously discussed in chapter 3. The sample time of the control pulses of each ideal switch is limited to equal values by the control block in the Simulink simulator. The limitation of the Simulink simulator does not prevent the production of the output voltage waveform of the inverter here.

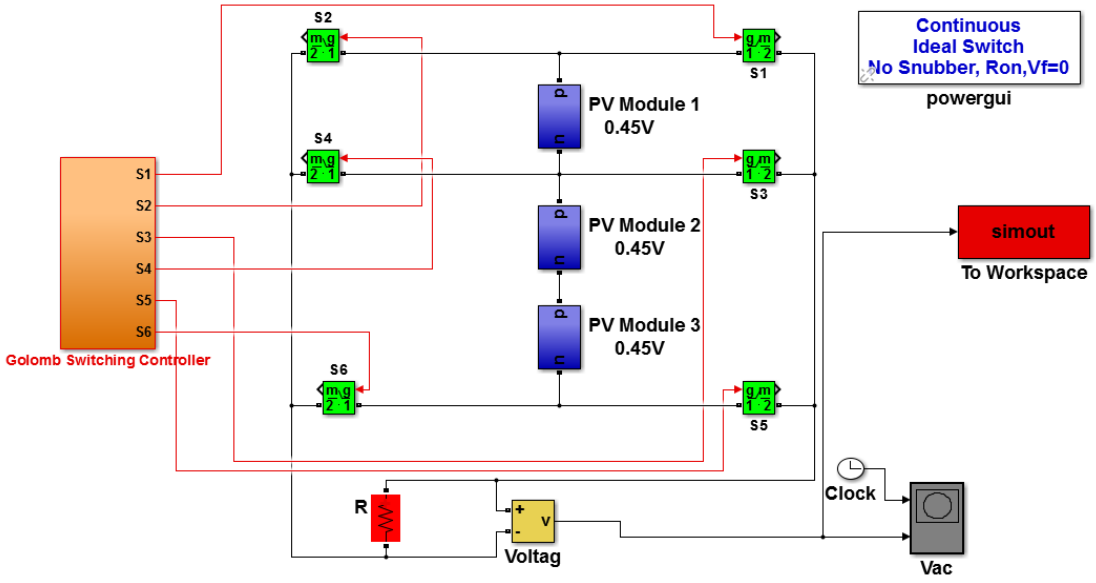

Figure 3.29: The complete 6 - level, Golomb multilevel inverter simulation setup

Figure 3.29 shows the complete single - phase, third - order based Golomb ruler multilevel inverter simulation setup. The three PV modules of 0.45 V each are the sources

of the conversion system here. Six ideal switches are used to switch on and switch off the PV modules according to the switching states. The voltage measurement block is used to measure the instantaneous voltage across the resistive load of 5kΩ for testing purposes. The output of the measurement block gives a Simulink signal that is captured through a Simulink Scope block clocks at the current simulation time. The controller block is implemented through the switching states table to form the switching pulses for both positive and negative half cycles as shown in Figure 3.30. The controller consists of repeating sequence stair masks that set the vector outputs of P1, P2, P3, P4, P5 and P6 to the switching states each at a sample time of 0.001666 s. These vectors are captured by a display through a multiplex vector signal bar (Mux block) of 6 inputs. The vector signals are passed through subsystem output ports (S1, S2, S3, S4, S5 and S6) to the ideal switches to form the required staircase voltage output waveform. The switching states of [S1, S2, S3, S4, S5, S6] are represented in arrays as: [100100], [001001], [100001], [100001], [001001],[100100], [011000],[000110],[010010],[010010], [000110] and [011000]. The sampling time (1.666 ms) for each vector signal is obtained by dividing one complete cycle period (20 ms) by the number of arrays.

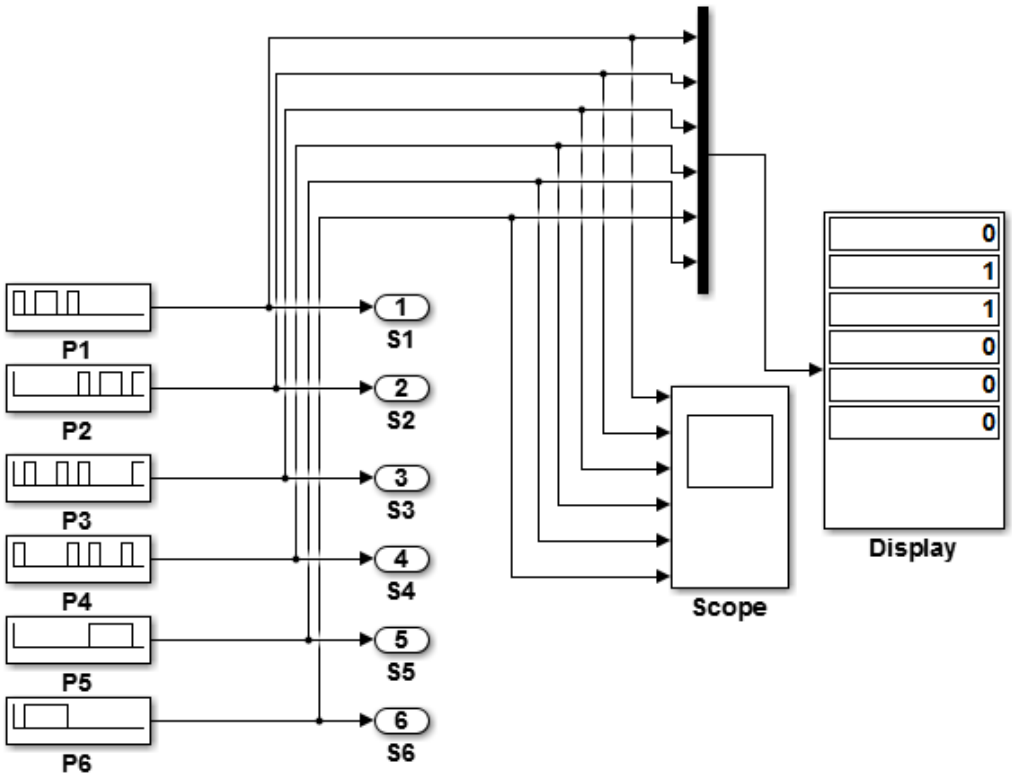

Figure 3.30: The layout of Golomb switching controller

To simulate any Simulink model containing SimPowerSystems specialized technology models, an environment block (powergui) is needed to run the simulation in a specific mode and gives a graphical user interface. The configuration of the solver tap in the powergui block is set to a continuous mode. The switching devices are also set through the solver tap to ideal in which snubbers, ON resistance (0 Ω) and forward voltage (0V) are all disabled.

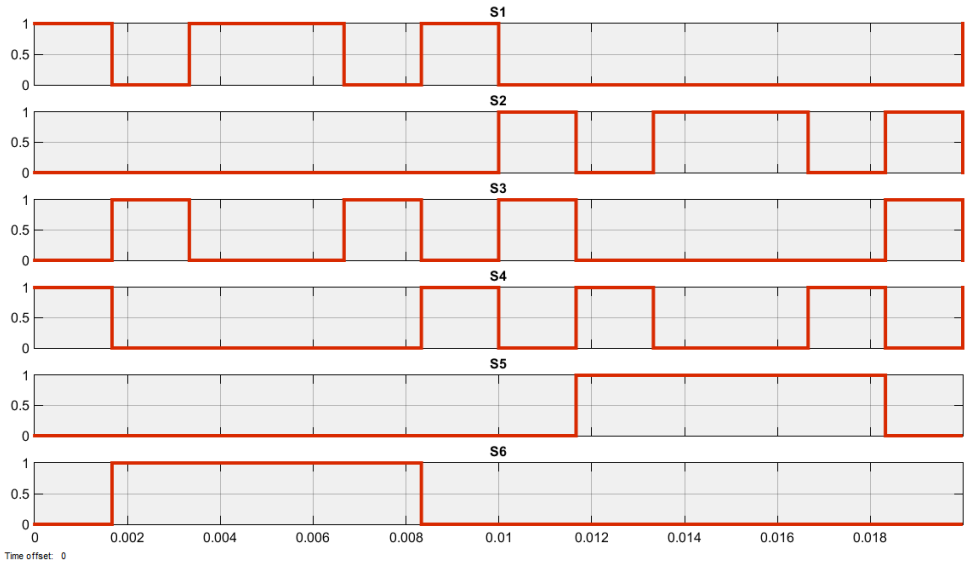

Figure 3.31: The simulated output waveform pulses of the Golomb controller that are fed to the ideal switches (One complete cycle)

Figure 3.31 shows the control waveform pulses for one complete cycle which is fed to the ideal switches. It is clear from the pulses that at any instant only two switches are conducting while the other switches are off. The output voltage waveform across the load and its fast Fourier transform FFT analysis for one complete cycle are captured through the powergui block as shown in Figure 3.32.

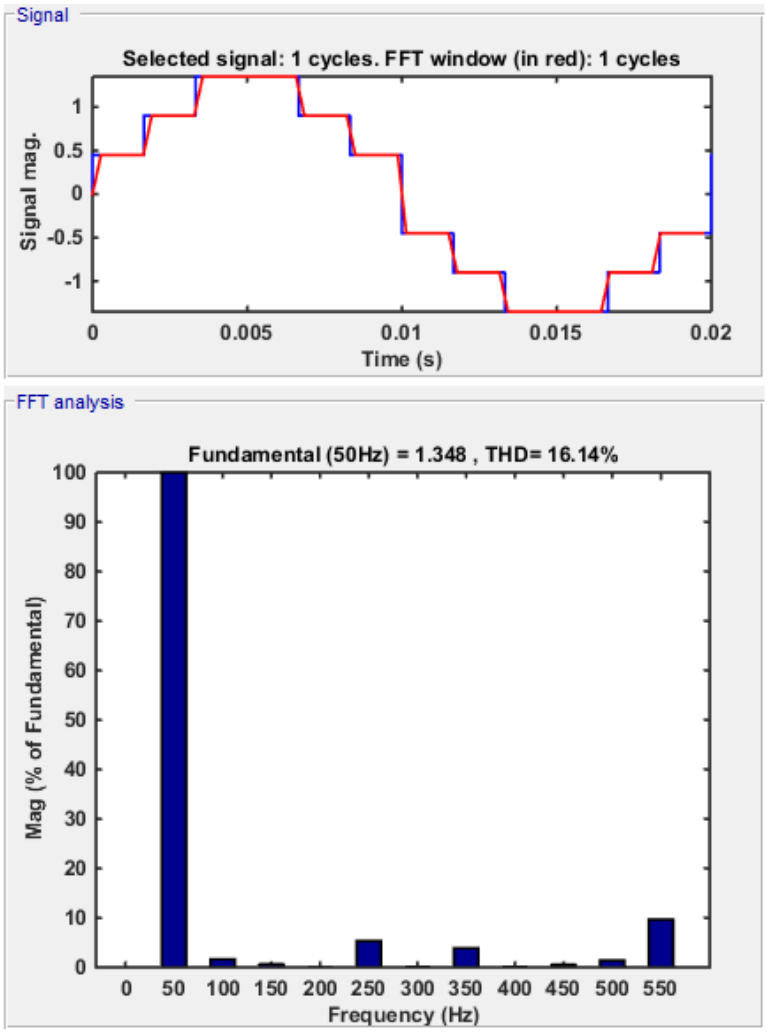

Figure 3.32: The simulated 6-level, Golomb voltage output waveform and FFT analysis

The peak voltage of the output waveform is 1.35 V which agrees well with the maximum expected from the input sources. It is very clear from Figure 3.32 that the fundamental frequency is 50 Hz. The simulation results shown in Figure 3.32 displays a 16.14% (-15.8 dB) total harmonic distortion (THD). The third harmonic component at (150 Hz) is approximately (0.5%) of the fundamental.

3.7.2 Third-order, DC-to-AC Golomb Multilevel inverter Experimental Prototype

The experimental prototype of the third-order, Golomb staircase direct conversion system is illustrated in Figure 3.33 and the complete description of the experimental setup is detailed in Chapter 3. C++ program code (Code is included in Appendix A) is applied to the Mbed microcontroller via the on-line complier where the timing steps of the output waveform (quarter cycle representation: $T_1 = 0.0016s$, $T_2 = 0.0017s$ and $T_3 = 0.0018s$) is set with respect to the heuristic technique (Chapter 3). The digital output pulses of each switch are hence generated according to the control switching of the inverter here at the selected pins of the microcontroller as illustrated in Figure 3.34 and Figure 3.35 (Note that the scope probes of MOSFET1, MOSFET3, MOSFET6 and MOSFET2 are set at 10). The code is designed such that any two consecutive time durations for the same output level is switched only once to avoid switching losses. For instance, the third positive output level is switched for double the time duration (3.6 ms) as shown in the code.

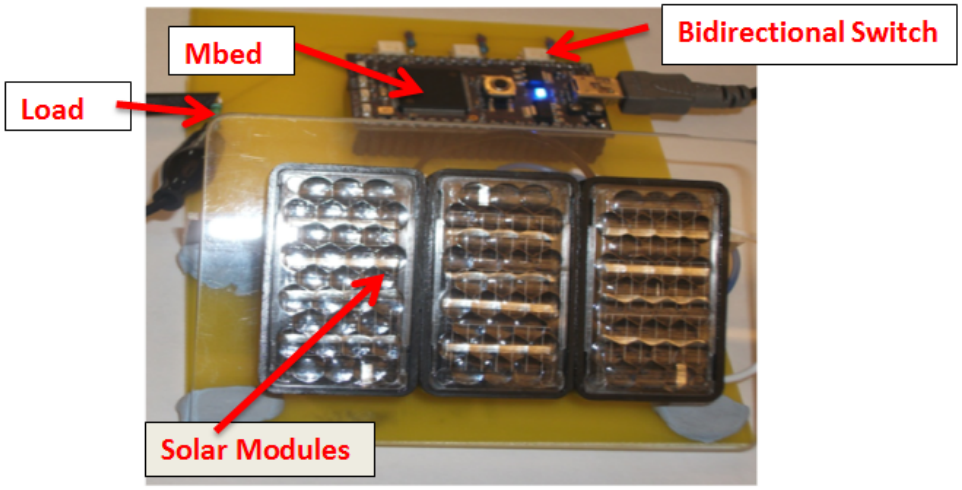

Figure 3.33: The experimental prototype of 6-level Golomb inverter

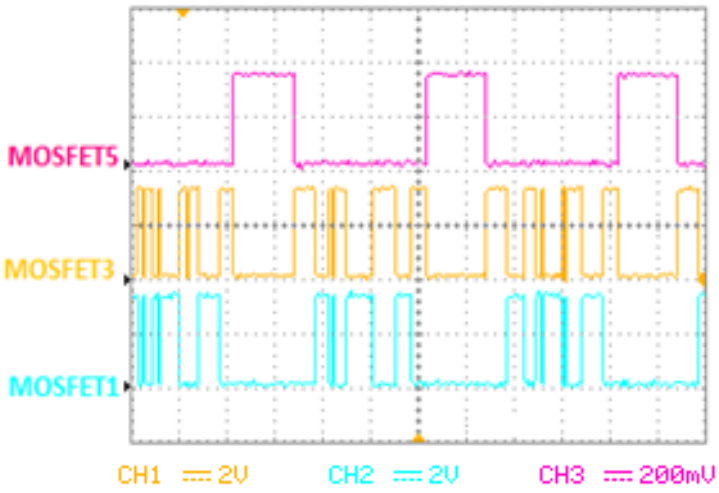

Figure 3.34: The experimental switching pulses for MOSFET1, MOSFET3 and MOSFET5

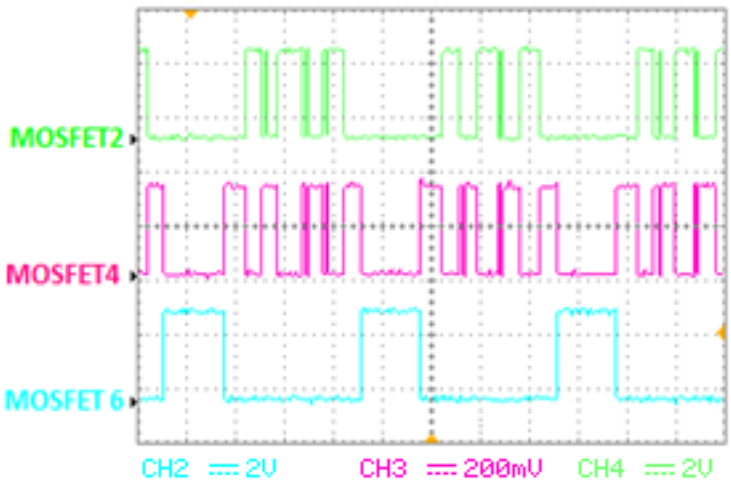

Figure 3.35: The experimental switching pulses for MOSFET2, MOSFET4 and MOSFET6

The output waveform is obtained across the resistive load of 10 kΩ by running the program code of the microcontroller as illustrated in Figure 3.36.

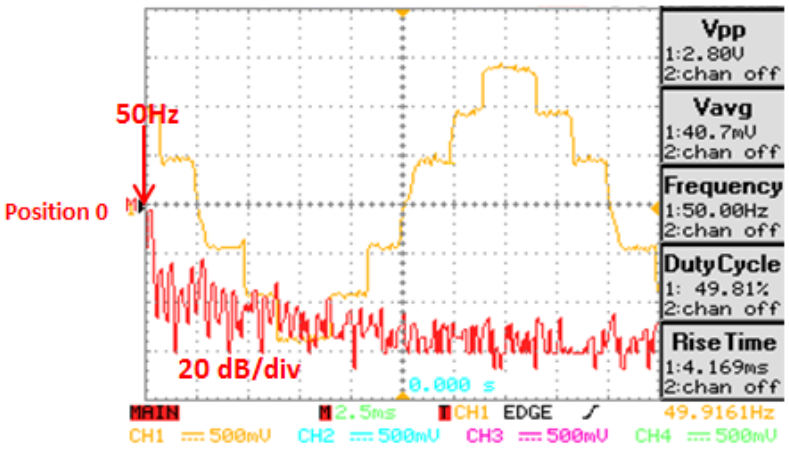

Figure 3.36: The experimental AC staircase output waveform of the third-order Golomb inverter and FFT spectrum

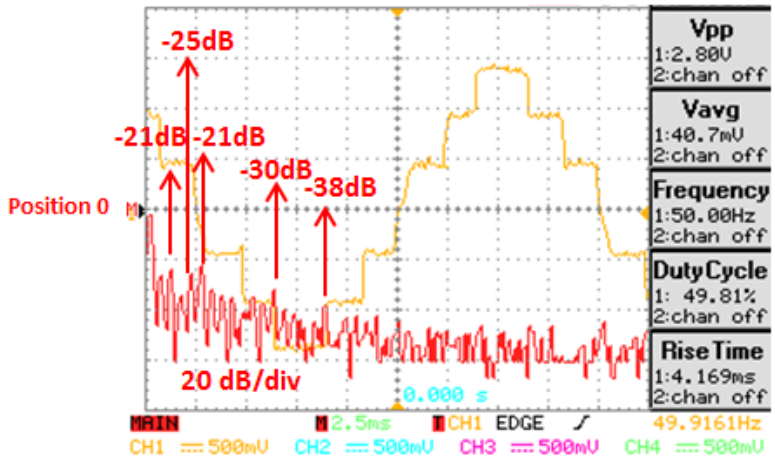

Figure 3.37: The significant harmonics in the FFT spectrum of the third-order Golomb inverter

It is clearly observable from the experimental results that the generated waveform is a 50 Hz stepping waveform with six different levels. This six - level inverter is hence highly practicable. The total harmonic distortion THD of the output signal is calculated by taking the root sum of the squares of the first five to six harmonics of the fundamental as given in equation (3.43).

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_z^2}}{V_{refn}} \tag{3.43}$$

where, V_z is in RMS voltage, and V_{refn} refers to the fundamental component of the voltage waveform in RMS.

The fundamental component of the output signal is marked on the spectrum in Figure 3.36 at (50 Hz) and the peak voltage of 1.4 V (approximately 1 V (RMS)). The first five significant harmonics of the output waveform here are noted as -21dB, -25dB, -21dB, -30dB and -38dB on the FFT spectrum in Figure 3.37. The values in dBs can

be to RMS voltage ratios using the well-known formula. Thus, the THD of the third-order Golomb inverter here is calculated using equation (3.43), resulting in 14.16% (-16.9 dB) THD.

3.8 Conclusion

This chapter presented a direct conversion, DC-to-AC six-level 50 Hz multilevel inverter for photovoltaic application based on the previously unexploited Golomb number theorems. The order selection of Golomb ruler presented is not confined to third-order perfect ruler; it can be adopted to any higher order optimum rulers at the expense of higher circuit complexity. Although here all the discussion relates to low power applications; it can be applied to higher power applications like in grid - connected inverters.

The major drawback of Golomb technique here is that the PV cells are not evenly utilized. As already discussed in section 3.5.3, the complete utilization of the PV cells is limited by Golomb ruler technique. The timing steps determination discussed in section 3.6.1 is based on a heuristic approach which is not practical for higher number of levels. However, there is an analogous variant of the inverter based on the cyclic selection theory that ensures even panel utilization. Additionally, the timing steps of the output signal is optimized using a new mathematical method which is presented in chapter 5. The cyclic selection inverter is discussed in the next chapter.

CHAPTER 4

CYCLIC SELECTION MULTILEVEL INVERTER

4.1 Introduction

It is seen in Chapter 2 that the complexity of conventional multilevel inverters increases dramatically as the number of level increases. Traditional magnetic-core PWM inverters typically synthesize the pure sine-wave voltage output waveform by varying the width of pulses. Problems of the PWM inverters are high voltage stresses, high losses and EMI. The high initial costs of the conventional PWM inverters have been

hindering their practical use in power generation systems [85]. It is also difficult for PWM inverters active filters to comply with EMI requirements. It is also discussed in Chapter 3 that Golomb structure causes uneven panel utilization issue. To solve these issues a novel cyclic selection inverter is proposed.

In this chapter, a novel single-phase, seven-level, cyclic selection, photovoltaic (PV) inverter which employs an H-bridge output stage incorporated with a cyclic selection type structure is presented. The need for magnetic materials is removed in this new topology by selecting series and parallel combinations of PV cells which ensures full panel utilization and produces a good-quality, sine-wave output signal. This topology in fact overcomes the redundancy in the DC sources and thus ensures they are evenly utilized. The proposed structure has the same performance as a conventional magmatic core-based PWM inverter. The cyclic selection technique allows on-panel battery provision such that a complete generation and storage module is realized.

The cyclic selection multilevel topology proposed here results in a reduction in the number of power switches and the configuration complexity. This topology features an ease of extension by increasing the number of segments and cascading them. Hence, the number of the output voltage levels increases and the inverter system expands.

4.2 Cyclic Selection Mathematical Theory and Comparisons

4.2.1 Description and Analysis of The Cyclic Selection Algorithm

The cyclic selection in this work can be defined as a combinational problem for selecting cyclically distinct subsets (n_{sub}) of identical elements out of a number of cyclic objects (X_{mn}). The cyclic selection technique was adopted as an optimization tool for designing a single-phase multilevel inverter that ensures full energy source utilization and produces a good-quality, sine-wave output signal by selecting series and parallel combinations of PV cells.

Given the total number of cyclic sources (X_{mn}), and the number of selected consecutive sources (n_{sub}), the proposed combinational problem is developed using a new simple but accurate mathematical model (Code is included on a CD). This model suits the user for any given number of sources (X_{mn}).

Considering that the number of (X_{mn}) is presented by a circular normal ruler with (X_{mn}) length and (X_{mn}) number of marks as illustrated in Figure 4.1.

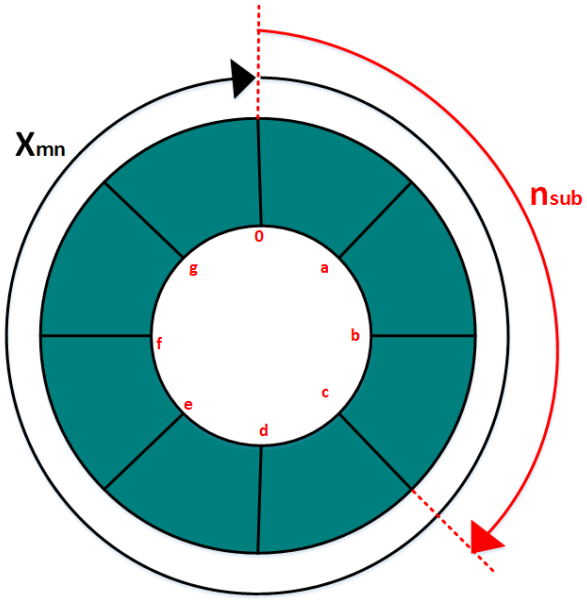

Figure 4.1: Circular ruler with (X_{mn}) length

The number of cycles of the selected number of sources (n_{sub}) from the maximum available ones (X_{mn}) is realized if the following conditions are met:

$$\begin{aligned} r_{mn} &\neq 0 \\ X_{mn} &> 2 \\ n_{sub} &\neq \{0, 1, X_{mn}\} \end{aligned} \tag{4.1}$$

The above notations in equation (4.1) indicate that the cyclic selection technique is realized when the maximum number of sources are greater than two, the remainder (r_{mn}) of the Euclidean division expressed in equation (4.3) is non zero and the selected number of sources (n_{sub}) is not equal to the following:

1. The maximum number of sources ($n_{sub} \neq X_{mn}$).

2. Zero ($n_{sub} \neq 0$) which means no selected source.

3. One object ($n_{sub} \neq 1$) which means one selected PV source.

$$X_{mn} = n_{sub} \times q_{mn} + r_{mn} \tag{4.2}$$

where q_{mn} is the quotient (positive integer), and r_{mn} is the remainder of the Euclidean division (positive integer) as expressed in equation (4.3).

$$\begin{aligned} r_{mn} &= X_{mn} \mod n_{sub} \\ n_{sub} &\neq \{0, 1, X_{mn}\} \end{aligned} \tag{4.3}$$

Denoting the number of cycles of the selected sources n_{sub} from the given maximum sources X_{mn} by cyc which can be expressed as in equation (4.4).

$$cyc = \frac{X_{mn}}{(GCF(F_{mn}, X_{mn} \mod F_{mn}))} - 1 \tag{4.4}$$

Thus, the total number of instances of loading the cells S_{mn} is greater than (cyc) by one value as given in equation (4.5).

$$S_{mn} = \frac{X_{mn}}{(GCF(F_{mn}, X_{mn} \mod F_{mn}))} \tag{4.5}$$

where GCF is the greatest common factor; $\mod$ is the modulo operation; F_{mn} is given by equation (4.6):

$$F_{mn} = X_{mn} - (X_{mn} \mod n_{sub}) \tag{4.6}$$

The number of instances S_{mn} is one when ($n_{sub} = 1$ or $n_{sub} = X_{mn}$ or $r_{mn} = 0$) as the sources will either appear in parallel or in series or parallel and series combinations

as detailed in the next section to ensure a complete panel utilization. A complete panel utilization here is the contribution of each employed PV cell to all the non-zero output DC levels of a multilevel signal.

4.2.2 Cyclic Selection Classifications

As mentioned in the previous section the cyclic selection technique is employed in this context as a design structure for a PV multilevel inverter to overcome the redundancy in the DC sources and thus ensures they are evenly utilized by selecting them in series or parallel combinations. This technique can be classified, for convenience, into three main categories reflecting the present and the absent of the cyclic technique within an inverter circuitry to produce the required output voltage level.

4.2.2.1 Non-Cyclic Configuration

As the name implies, this configuration requires no cycling to the cells to produce the desired voltage from the selected number of sources. This can be categorized into three groups, reflecting the connection appearance of the PV sources in the inverter circuitry.

4.2.2.1.1 Series Structure

In this category, all the DC sources connected in the inverter circuitry appear as a series connection. In other words, all the DC sources are connected in series. This category is only realized when the number of selected sources is equal to the maximum

given DC sources and thus $r_{mn} = 0$ & $q_{mn} = 1$ in equation (4.2). Equation (4.2) can be rewritten in this case as:

$$X_{mn} = n_{sub} \tag{4.7}$$

Assuming that each PV cell has a voltage of V_{mn}, the maximum available voltage V_{mmMax} from X_{mn} sources is given by equation (4.8).

$$V_{mmMax} = X_{mn} \times V_{mn} \tag{4.8}$$

Consequently, the selected voltage $V_{mmSelec}$ from the PV cells becomes:

$$V_{mmSelec} = n_{sub} \times V_{mn} \tag{4.9}$$

Using the property of the series structure in (4.7), it is possible to conclude that $V_{mmSelec} = V_{mmMax}$.

For example, taking X_{mn} and n_{sub} in Figure 4.1 as 4 sources to illustrate the series configuration of the non-cyclic technique. A_{mn}, B_{mn}, C_{mn} and D_{mn} are assumed to be PV cells with 1 V each as an example.

Thus,

$$V_{mmMax} = 4 \text{ V} \tag{4.10}$$

$$V_{mmSelec} = 4 \text{ V} \tag{4.11}$$

Therefore, the selection of $n_{sub} = 4$ out of $X_{mn} = 4$ to generate a 4 V output is achieved by connecting all the sources in series $(A_{mn} + B_{mn} + C_{mn} + D_{mn})$ as shown in Table 4.1 and Figure 4.2. It can be deduced from Figure 4.2 that all sources are utilized evenly as a series combination to produce the required voltage output level.

Table 4.1: $X_{mn} = 4$ & $n_{sub} = 4$

PV cells	A_{mn}	B_{mn}	C_{mn}	D_{mn}
S_{mn}	1	1	1	1

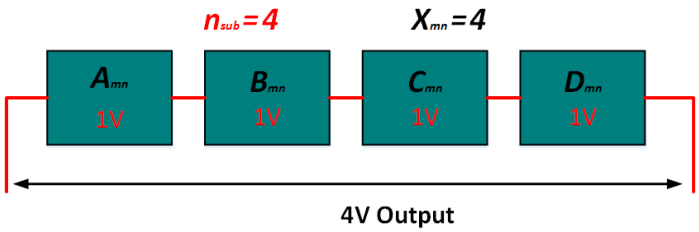

Figure 4.2: Ruler with $X_{mn} = 4$ and $n_{sub} = 4$

Table 4.1 illustrates that all the DC cells are evenly utilized $S_{mn} = 1$ and they appear as a series connection. Additionally, it is observed from this example that $cyc = 0$ which means that the cycle technique is not required to produce the maximum voltage from all the cells.

As another example of series configuration, let us assume that the maximum number of given sources is $X_{mn} = 10$ and the selected ones are 10 sources ($n_{sub} = 10$); using the same PV cell information given in the previous example, it is found that the maximum available voltage from the cells is produced by connecting all the cells in series as shown in Figure 4.3.

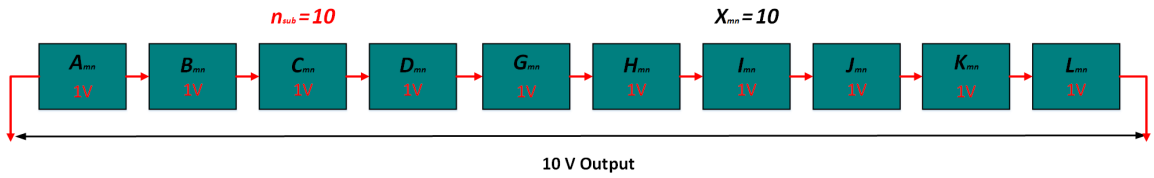

Figure 4.3: Ruler with $X_{mn} = 10$ and $n_{sub} = 10$

Consequently, the number of instances that each cell is loaded to produce the maxi-

mum voltage is one as shown in Table 4.2.

Table 4.2: $X_{mn} = 10$ & $n_{sub} = 10$

PV cells	A_{mn}	B_{mn}	C_{mn}	D_{mn}	G_{mn}	H_{mn}	I_{mn}	J_{mn}	K_{mn}	L_{mn}
S_{mn}	1	1	1	1	1	1	1	1	1	1

4.2.2.1.2 Parallel Structure

In this category, all the DC sources connected in the inverter circuitry appear as a parallel connection. This category is only realized when $r_{mn} = 0$ & $n_{sub} = 1$ in equation (4.2). Equation (4.2) can be rewritten in this case as:

$$X_{mn} = q_{mn} \tag{4.12}$$

Assuming that each PV cell has a voltage of V_{mn}, the minimum voltage V_{mmMin} from X_{mn} sources is given by equation (4.13).

$$V_{mmMin} = V_{mn} \tag{4.13}$$

Comparing equation(4.13) with equation (4.8), one can see that $V_{mmMin} = V_{mmMax}$ when $X_{mn} = 1$ which refers to one PV source scenario. For a given number of PV sources X_{mn}, where $X_{mn} \neq 0, 1$; one may claim that the minimum voltage from the available cells equals one PV cell voltage ($V_{mmMin} = V_{mn}$) is only realized when all the sources appear in parallel.

The selected voltage $V_{mmSelec}$ from the PV cells in this case can be written as:

$$V_{mmSelec} = n_{sub} \times V_{mn} \tag{4.14}$$

Using the property of the parallel structure in (4.12), equation (4.14) can be rewritten as:

$$V_{mmSelec} = V_{mn} \tag{4.15}$$

Comparing equation (4.15) with equation (4.13), it may be observed that $V_{mmSelec} = V_{mmMin}$ in the parallel structure case.

To illustrate an example of the parallel configuration of the non-cyclic technique, we take (X_{mn}) in Figure 4.1 as 5 sources and we select $n_{sub} = 1$. Here, it is assumed that A_{mn}, B_{mn}, C_{mn}, D_{mn} and G_{mn} are PV panels of 3 V each as an example.

Thus,

$$V_{mmMin} = 3 \text{ V} \tag{4.16}$$

$$V_{mmSelec} = 3 \text{ V} \tag{4.17}$$

Therefore, selecting $n_{sub} = 1$ out of $X_{mn} = 5$ and utilizing all the sources to generated 3 V output are achieved by paralleling all the sources $(A_{mn}||B_{mn}||C_{mn}||D_{mn}||G_{mn})$ as shown in Table 4.3 and Figure 4.4.

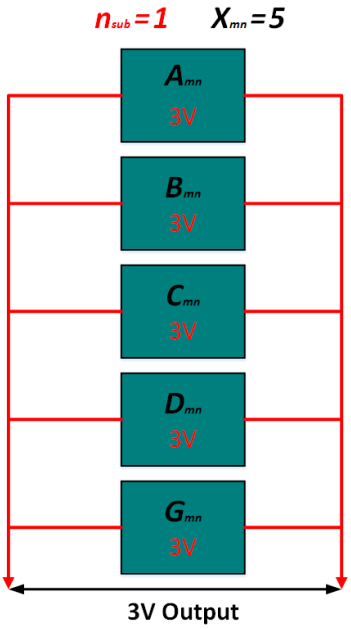

Figure 4.4: Ruler with $X_{mn} = 5$ and $n_{sub} = 1$

Table 4.3: $X_{mn} = 5$ & $n_{sub} = 1$

PV cells	A_{mn}	B_{mn}	C_{mn}	D_{mn}	G_{mn}
S_{mn}	1	1	1	1	1

Table 4.3 illustrates that all the DC cells are evenly utilized $S_{mn} = 1$ as a parallel combination and thus $cyc = 0$ which means that the cyclic technique is not required to produce the minimum voltage from all the cells.

4.2.2.1.3 Series-Parallel Structure

In this category, the DC sources connected in the inverter circuitry appear as series and parallel combinations. This is only realized when ($r_{mn} = 0$ & $\frac{X_{mn}}{n_{sub}} > 1$) in

equation (4.2). Equation (4.2) can be rewritten in this case as:

$$X_{mn} = q_{mn} \times n_{sub} \tag{4.18}$$

Assuming that each PV cell has a voltage of V_{mn} and thus the selected voltage $V_{mmSelec}$ from the PV cells in this case can be written as:

$$V_{mmSelec} = n_{sub} \times V_{mn} \tag{4.19}$$

To show an example of the series - parallel configuration of the non - cyclic technique, we take (X_{mn}) as 6 sources and we select $n_{sub} = 2$. It is assumed that A_{mn}, B_{mn}, C_{mn}, D_{mn}, E_{mn} and N_{mn} are PV panels of 2 V each as an example.
Thus,

$$V_{mmSelec} = 4 \text{ V} \tag{4.20}$$

Therefore, selecting $n_{sub} = 2$ out of $X_{mn} = 6$ and utilizing all the sources to generate a 4 V output are achieved by connecting each consecutive pair of PV cells in series and then paralleling them as shown in Figure 4.5. The beauty of the switching control of the cyclic selection circuit is that the cells can appear in different combinations. Thus, the cells appear in this example as:

$$((A_{mn} + B_{mn})||(C_{mn} + D_{mn})||(E_{mn} + N_{mn})$$

or:

$$((N_{mn} + A_{mn})||(B_{mn} + C_{mn})||(D_{mn} + E_{mn})$$

The number of instances S_{mn} is one in this case and $cyc = 0$ thus the cells are evenly utilized as a series and parallel combinations.

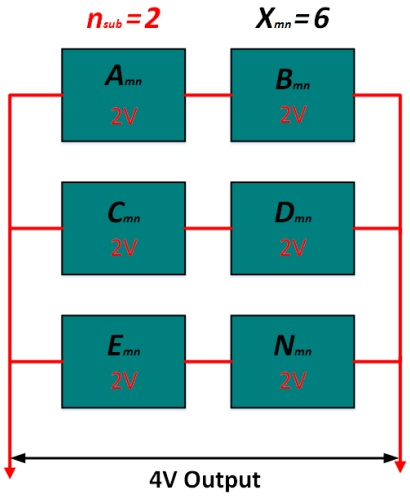

Figure 4.5: Ruler with $X_{mn} = 6$ and $n_{sub} = 2$

4.2.2.2 Cyclic Configuration (Shuffle)

This configuration requires cycling of the cells to produce the desired voltage from the selected number of sources. The cyclic technique is adopted in this work to overcome the redundancy in DC sources and ensure they are evenly utilized. This technique allows a time sharing to produce a particular voltage from a given maximum number of cells X_{mn}. The control switching strategy of the proposed inverter here ensures a complete panel utilization.

The cyclic technique is realized if (4.1) is valid. For instance, taking $n_{sub} = 3$ & $X_{mn} = 4$; resulting in $r_{mn} = 1$ from equation (4.3) and $cyc = 3$ from equation (4.4). Assuming that four PV panels with batteries of 2.5 V each are used as an example (denoting as A_{mn}, B_{mn}, C_{mn} and D_{mn}) and an output voltage level of 7.5 V is required. The cyclic technique is applied in this case as shown in the cyclic mapping in Table 4.4.

Table 4.4: $X_{mn} = 4$ & $n_{sub} = 3$

A_{mn}	B_{mn}	C_{mn}	D_{mn}
1	1	1	0
1	2	2	1
2	2	3	2
3	3	3	3

Table 4.4 can be expressed in terms of the connections appearance of the cells in each row as:

$$S_{mn} \begin{cases} (1,1,1,0) \Rightarrow A_{mn} + B_{mn} + C_{mn} \\ (1,2,2,1) \Rightarrow B_{mn} + C_{mn} + D_{mn} \\ (2,2,3,2) \Rightarrow A_{mn} + C_{mn} + D_{mn} \\ (3,3,3,3) \Rightarrow A_{mn} + B_{mn} + D_{mn} \end{cases} \tag{4.21}$$

It is noticeable from (4.21) that the total number of instances the panels are utilized is $S_{mn} = 4$. The summation terms in (4.21) are the series connection of the panels at each instance for the selected output voltage (3 out of 4 in this case). Therefore, the cells A_{mn}, B_{mn} and C_{mn} in $(1,1,1,0)$ are connected in series for the first time. It is true that D_{mn} is not connected to generated the selected voltage at this instance as shown in Figure 4.6 but it is charging the battery to ensure full panel utilization. Furthermore, B_{mn}, C_{mn} panels are connected in series in $(1,2,2,1)$ for the second time while D_{mn} is connected in series for the first time and A_{mn} is not connecting at this instance as shown in Figure 4.7. Yet, A_{mn} is charging the battery at this instance. In $(2,2,3,2)$, A_{mn} and D_{mn} are connected in series for the second time while C_{mn} is connected in series for the third time and B_{mn} is not connecting at this instance as shown in Figure 4.8 but it is charging the battery. In $(3,3,3,3)$, A_{mn}, B_{mn} and D_{mn} are connected in series for the third time while C_{mn} is not connected but it is charging

the battery at this instance as shown in Figure 4.9. The shuffle (cyclic) technique to the cells in a circular direction is clearly realized in this example. In fact, the cells are shuffled three times $cyc = 3$ as in the following notations:

$$\left.\begin{aligned} (1,2,2,1) &\Rightarrow B_{mn} + C_{mn} + D_{mn} \\ (2,2,3,2) &\Rightarrow A_{mn} + C_{mn} + D_{mn} \\ (3,3,3,3) &\Rightarrow A_{mn} + B_{mn} + D_{mn} \end{aligned}\right\} cyc$$

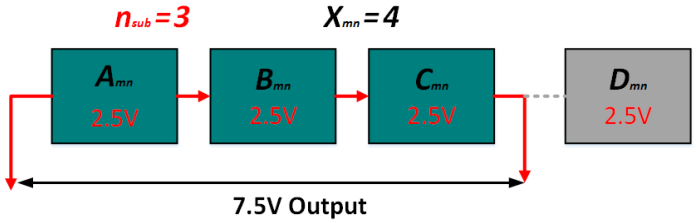

Figure 4.6: Ruler with $X_{mn} = 4$ and $n_{sub} = 3$

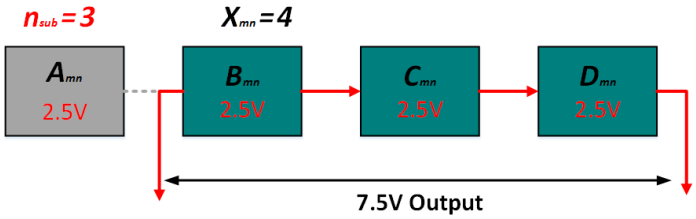

Figure 4.7: Ruler with $X_{mn} = 4$ and $n_{sub} = 3$

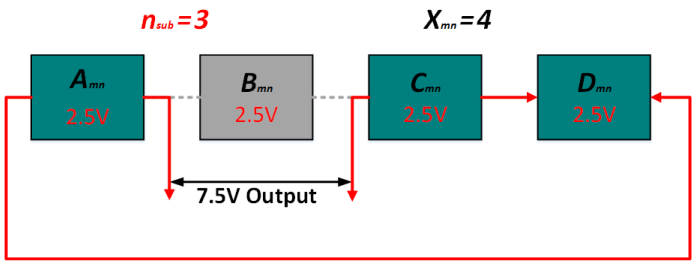

Figure 4.8: Ruler with $X_{mn} = 4$ and $n_{sub} = 3$

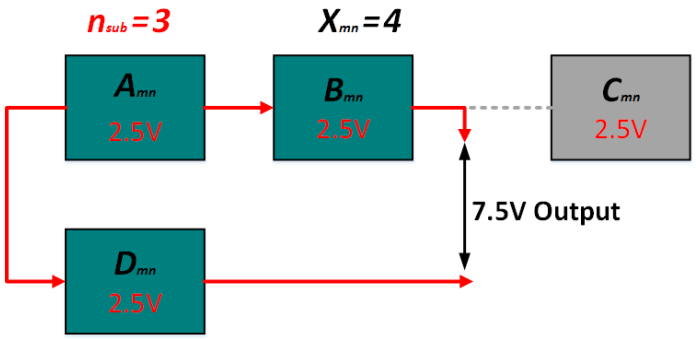

Figure 4.9: Ruler with $X_{mn} = 4$ and $n_{sub} = 3$

Another shuffle example is presented here by taking $X_{mn} = 15$ and $n_{sub} = 7$ and the analysis is illustrated in Table 4.5. The cells are clearly shuffled 14 times in this example and 15 instances the cells are loaded. The combinations of the cells in this case are a mixture of parallel and series connection. Thus, choosing 7 out of 15 can be expressed as $(A_{mn}+B_{mn}+C_{mn}+D_{mn}+E_{mn}+G_{mn}+H_{mn}||\ I_{mn}+J_{mn}+K_{mn}+L_{mn}+M_{mn}+N_{mn}+O_{mn})$ which indicates the fact 7 cells can be found twice out of 15 with 1 remainder as shown in the first row $(1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 0)$ of Table 4.5. In other words, each row of the table presents seven series cells that are in parallel connection with another seven cells while one cell is left out until the next instance. However, the single cell that has left out at each state is charging a battery.

Table 4.5: $X_{mn} = 15$ & $n_{sub} = 7$

A_{mn}	B_{mn}	C_{mn}	D_{mn}	E_{mn}	G_{mn}	H_{mn}	I_{mn}	J_{mn}	K_{mn}	L_{mn}	M_{mn}	N_{mn}	O_{mn}	P_{mn}
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	2	2	2	2	2	2	2	2	2	2	2	2	2	1
2	2	3	3	3	3	3	3	3	3	3	3	3	3	2
3	3	3	4	4	4	4	4	4	4	4	4	4	4	3
4	4	4	4	5	5	5	5	5	5	5	5	5	5	4
5	5	5	5	5	6	6	6	6	6	6	6	6	6	5
6	6	6	6	6	6	7	7	7	7	7	7	7	7	6
7	7	7	7	7	7	7	8	8	8	8	8	8	8	7
8	8	8	8	8	8	8	8	9	9	9	9	9	9	8
9	9	9	9	9	9	9	9	9	10	10	10	10	10	9
10	10	10	10	10	10	10	10	10	10	11	11	11	11	10
11	11	11	11	11	11	11	11	11	11	11	12	12	12	11
12	12	12	12	12	12	12	12	12	12	12	12	13	13	12
13	13	13	13	13	13	13	13	13	13	13	13	13	14	13
14	14	14	14	14	14	14	14	14	14	14	14	14	14	14

4.2.2.3 Shortcut Configuration

The shortcut approach is realized in the cyclic selection problem at certain conditions. The beauty of this technique is that it allows the use of an unlimited number of DC sources (X_{mn}) and minimizes the computation time. This technique is valid for the cyclic configurations ($r_{mn} \neq 0$) if one of the following conditions is met:

1. An equivalent fraction to $\frac{X_{mn}}{n_{sub}}$ is found and $q_{mn} = 1$. Hence, the cells are shuffled and appear as a series connection.

2. Quotient q_{mn} in equation (4.2) is greater than 1 and an equivalent fraction to $\frac{X_{mn}}{n_{sub} \times q_{mn}}$ is found. Hence, the cells are shuffled and they appear as a mixture of series and parallel combinations.

This technique is defined here as a shorter root that minimizes the number of cycles *cyc* and the number of instances S_{mn}. Taking X_{mn} as 15 and 24 as examples to

analyse the shortcut technique in both cases odd and even number of sources. Figure 4.10 and Figure 4.11 show the number of instances at which the panels are utilized to produce the required voltage output levels. In fact, each voltage selection n_{sub} out of the maximum available sources X_{mn} contributes to an output level. For example, the selection of 4 out of 15 generates the fourth level of the output signal.

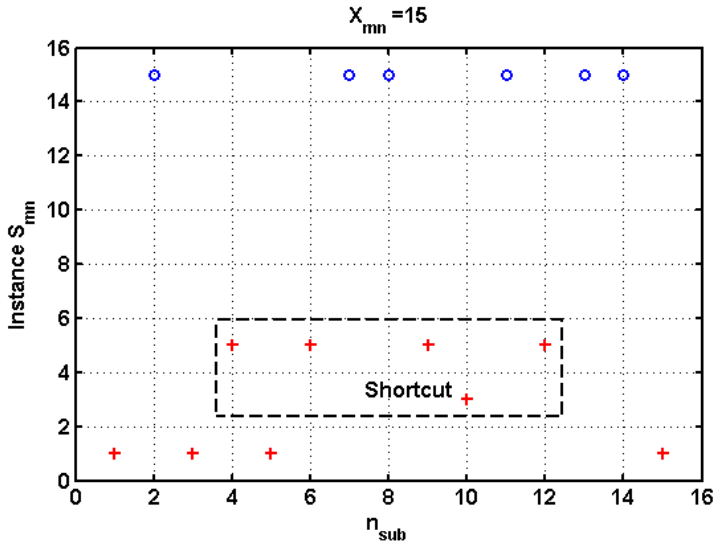

Figure 4.10: The number of instances at n_{sub}=1 to 15 at $X_{mn} = 15$

It is clear from Figure 4.10 that the number of instances of loading the cells when $n_{sub} = 4, 6, 9, 10$ and 12 is minimized as the conditions of the shortcut technique are realized. It is realized that the number of instances is 5 when $n_{sub} = 4$ due to the fact that it is possible to connect 12 cells with four in series at each instance and then parallel them. The unutilized cells for the first instance however are shuffled in a circular direction till the balancing is achieved. One can claim that the total number of instances the cells are loaded in the case of 10 out of 15 is equivalent to 2 out of 3. The mapping table of 2 out of 3 is illustrated in Table 4.6.

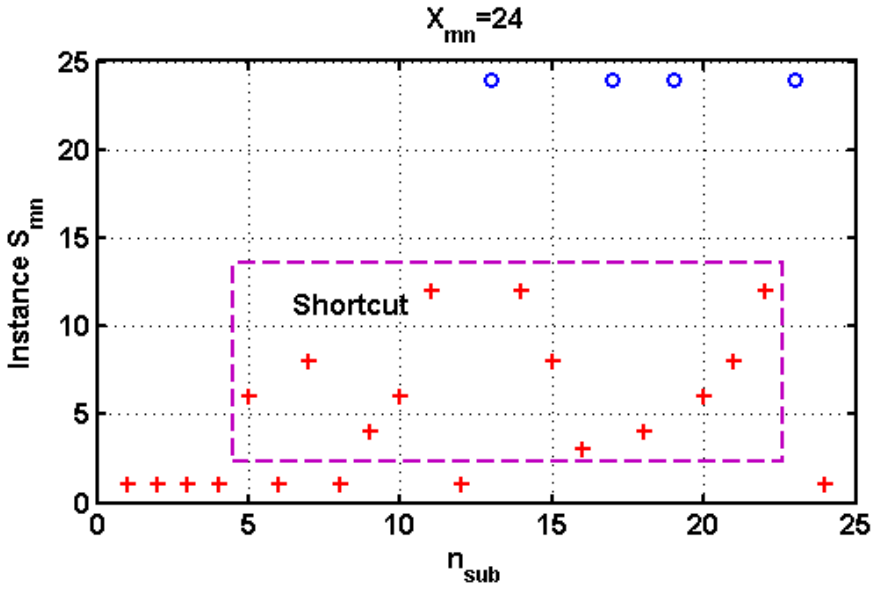

Figure 4.11: The number of instances at n_{sub}=1 to 24 at $X_{mn} = 24$

Table 4.6: $X_{mn} = 3$ & $n_{sub} = 2$

A_{mn}	B_{mn}	C_{mn}
1	1	0
1	2	1
2	2	2

It can be concluded from Table 4.6 that the number of instances of loading the cells is three where each individual cell is utilized twice. Thus, cell A_{mn} is utilized twice in the first and the last instances while it is not used in the second instance. However, A_{mn} is charging a battery at the second instance.

It can be observed from Figure 4.10 that the number of instances when $n_{sub} = 4$ and 6 is equal as both satisfy the second criteria of the shortcut technique:

$$\begin{aligned} (n_{sub} = 4) &\Rightarrow \frac{15}{4+4+4} = \frac{15}{12} \equiv \frac{5}{4} \\ (n_{sub} = 6) &\Rightarrow \frac{15}{6+6} = \frac{15}{12} \equiv \frac{5}{4} \end{aligned} \tag{4.22}$$

One can claim that the number of instances is also 5 when $n_{sub} = 9$ and $n_{sub} = 12$ in this example as both satisfy the first criteria of the shortcut technique.

$$\begin{aligned} (n_{sub} = 9) &\Rightarrow \frac{15}{9} \equiv \frac{5}{3} \\ (n_{sub} = 12) &\Rightarrow \frac{15}{12} \equiv \frac{5}{4} \end{aligned} \tag{4.23}$$

The shortcut technique of $X_{mn} = 24$ appears at ($n_{sub} = 5, 7, 9, 10, 11, 14, 15, 16, 18, 20, 21,$ and 22). The total number of instances of loading the cells when $n_{sub} = 5, 10$ and 20 is 6 due to the following criteria:

$$\begin{aligned} (n_{sub} = 5) &\Rightarrow \frac{24}{5+5+5+5} = \frac{24}{20} \equiv \frac{6}{5} \\ (n_{sub} = 10) &\Rightarrow \frac{24}{10+10} = \frac{24}{20} \equiv \frac{6}{5} \\ (n_{sub} = 20) &\Rightarrow \frac{24}{20} \equiv \frac{6}{5} \end{aligned} \tag{4.24}$$

The numerators at $n_{sub} = 5, 10$ indicate to the appearance combinations of the cells, for instance, the combination of $5+5+5+5$ indicates that each available 5 cells up to 20 cells are firstly connected in series. The resulting four series combinations of five cells each are then paralleled. The remaining four cells are then shuffled to satisfy the fair usage of the cells. Thus, the notations of $n_{sub} = 5$ and 10 can be expressed as:

$$\begin{aligned} (n_{sub} = 5) &\Rightarrow \frac{24}{5_{series}||5_{series}||5_{series}||5_{series}} \\ (n_{sub} = 10) &\Rightarrow \frac{24}{10_{series}||10_{series}} \end{aligned} \tag{4.25}$$

It can be concluded from the shortcut analysis that the cyclic selection method can also be applied to higher orders.

4.2.3 Circular Golomb Rulers and Modular Golomb - Sparse - Wichmann Rulers

The previous sections describe how circular rulers can be exerted for designing a multilevel inverter. One can show that circular rulers are well documented in literature in a form of a modular Golomb ruler and a circular sparse ruler [86, 87], [88]. A circular Golomb is thought of as wrapping around a linear near-optimal construction Golomb ruler as shown in Figure 4.12.

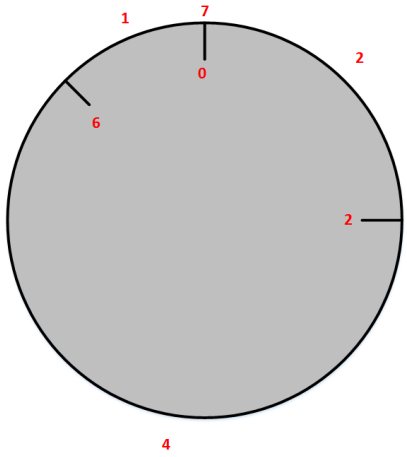

Figure 4.12: Modular Golomb ruler of 3 marks

Figure 4.12 shows a modular Golomb of three marks at which all the distances from 0 to 7 can be measured unlike the linear version of (0,2,6,7) where length 3 can not be measured. The beauty of a modular Golomb is that it allows a perfect distance set with fewer number of taps than the linear version as clearly shown in the previous example. It is worth noting that not every linear Golomb ruler can be a modular Golomb ruler.

However, a linear sparse ruler is defined as a ruler in which few of the distance marks

may be missing. In other words, this ruler measures all distances up-to its full length with the possibility of repeating some of them. For example, there is two well-known configurations of the linear sparse ruler with 4 marks of length 5; one is $(0, 1, 2, 5)$ and $(0, 1, 3, 5)$ in which all distances from (0 to 5) are measured. In $(0, 1, 2, 5)$, distance 1 can be taken between the marks (0,1) or (1,2). In contrast, distance 2 in $(0, 1, 3, 5)$ can be taken between the marks (1,3) or (3,5). Additionally, the circular sparse rulers can be defined as wrapping around a linear sparse ruler. Taking the previous linear sparse ruler $(0, 1, 2, 5)$ as an example to construct a circular one as depicted in Figure 4.13.

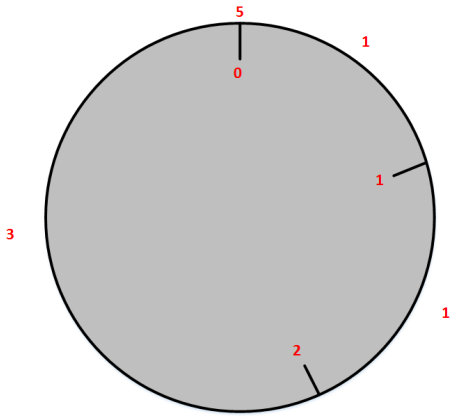

Figure 4.13: Modular sparse ruler of 3 marks

This modular ruler measures all possible distances from 0 to 5 similar to its linear version. However, length 4 can be measured between two different taps: between the marks 1 and 5 in a clockwise direction or between the marks 1 and 2 in anti-clockwise. Further, a Wichmann ruler $W_{r,s}$ is an optimal (perfect) linear sparse ruler which has a length of $w_{r,s} = 4r(r+s+2)+3(s+1)$ with exactly $4r+s+3$ number of marks [89]. The Wichmann ruler of $r > 0$ & $s > 0$ has difference representation of $[(1^r,\ r+1,\ (2r+1)^r,\ (4r+3)^s,\ (2r+2)^{(r+1)},\ 1^r)]$ [90]. For instance, $W(1, 1)$ is represented by:

- 1 distance of length 1
- 1 distance of length 2
- 1 distance of length 3
- 2 distances of length 4
- 1 distance of length 7
- 1 distance of length 1

It is observed that this Wichmann ruler $W(1,1)$ has exactly 8 marks with length of 22. However, there are nine different configurations of sparse rulers of length 22 with 8 marks. According to the Wichmann ruler representation distances above, we deduce that $[0,1,3,6,13,17,21,22]$ is the only Wichmann ruler among all the available sparse rulers of the same length and number of marks. It can be observed from the representations $[(2r+1)^r, (4r+3)^s, (2r+2)^{(r+1)}]$ of Wichmann rulers that some of the middle segments are repeated. This observation allows the reconstruction of a perfect Golomb-sparse-Wichmann ruler based on the modular Golomb ruler. The latter was shown previously in Figure 4.12.

The new circular Golomb-sparse-Wichmann ruler $G_{SW}(r_{gsw}, s_{gsw})$ has different representations of $[2^{(1+s_{gsw})}, 4^{r_{gsw}}, 1^{s_{gsw}}]$ of $(4r_{gsw}+s_{gsw}+3)$ length and $(2+r_{gsw})$ marks. The original modular Golomb ruler discussed previously can be seen as $G_{SW}(1,0)$ of length 7 with 3 marks. $G_{SW}(3,0)$ has 5 marks with the length 15 as shown in Figure 4.14.

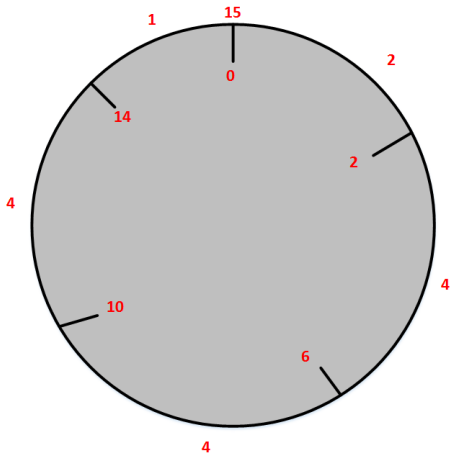

Figure 4.14: Modular Golomb-sparse-Wichmann Ruler of 5 marks

It is worth noting that the number of taps increases as r_{gsw} rises. Thus, $G_{SW}(6,0)$ has 8 marks with the length 27. This new ruler is compared with the well-known linear Wichmann sparse rulers with the same number of marks as illustrated in Table 4.7.

Table 4.7: The comparisons between modular Golomb-sparse-Wichmann rulers and linear Wichmann-sparse rulers

Marks	Length of Modular $G_{SW}(r_{gsw}, s_{gsw})$	Length of Linear $W(r,s)$
3	$7 \Rightarrow G_{SW}(1,0)$	$3 \Rightarrow W(0,0)$
4	$11 \Rightarrow G_{SW}(2,0)$	$6 \Rightarrow W(0,1)$
5	$15 \Rightarrow G_{SW}(3,0)$	$9 \Rightarrow W(0,2)$
6	$19 \Rightarrow G_{SW}(4,0)$	$12 \Rightarrow W(0,3)$
7	$23 \Rightarrow G_{SW}(5,0)$	$15 \Rightarrow W(0,4)$ & $W(1,0)$
8	$27 \Rightarrow G_{SW}(6,0)$	$18 \Rightarrow W(0,5)$
9	$31 \Rightarrow G_{SW}(7,0)$	$29 \Rightarrow W(1,2)$
10	$35 \Rightarrow G_{SW}(8,0)$	$36 \Rightarrow W(1,3)$

It can be concluded from the table that the new developed ruler with fewer marks up to 9 taps can produce a higher length than the conventional linear Wichmann rulers. Applying the switching ladder topology discussed in Chapter 3 to the modular Golomb-

sparse-Wichmann ruler in Figure 4.14 with a breakage switch to avoid a short circuit across the output terminal. For example, the 5^{th} order ruler Golomb-sparse-Wichmann topology can be structured with 1 V PV cells and five taps only (10 bidirectional switches) in which all the possible voltage levels from 0 to 14 V can be generated. One tap (two switches) is saved in this modular topology with higher levels compared to the linear version.

4.3 A Multilevel DC to AC Cyclic Selection Inverter for Photovoltaic Application

4.3.1 The Operation Principle of a Single - phase, Seven - Level, Cyclic Selection Multilevel Inverter

This section explains the principles of a single-phase, 7-level, cyclic selection, DC-to-AC staircase inverter for PV applications. The proposed inverter has a single H-bridge stage with three segments. Importantly, the H-bridge stage inverts the voltage levels from positive to negative which are produced by the level cyclic circuit. The latter is designed to produce the selected level voltages from the sources. It is worth noting that each segment in the level cyclic circuit consists of two diodes, a DC source and a semiconductor switching device. A 7-level inverter requires three MOSFET switches in the level cycle circuit ($S_{cyc_1}, S_{cyc_2}, S_{cyc_3}$) connected to three DC sources (PV panels with batteries) of equal voltages ($V_{cyc_1} = V_{cyc_2} = V_{cyc_2} = V_{dc-cyc}$) with six diodes ($D_{cyc_1}, D_{cyc_2}, D_{cyc_3}, D_{cyc_4}, D_{cyc_5}, D_{cyc_6}$). The use of high speed and low

forward voltage drop diodes for this topology is essential. The equivalent circuit of the proposed inverter is given in Figure 4.15.

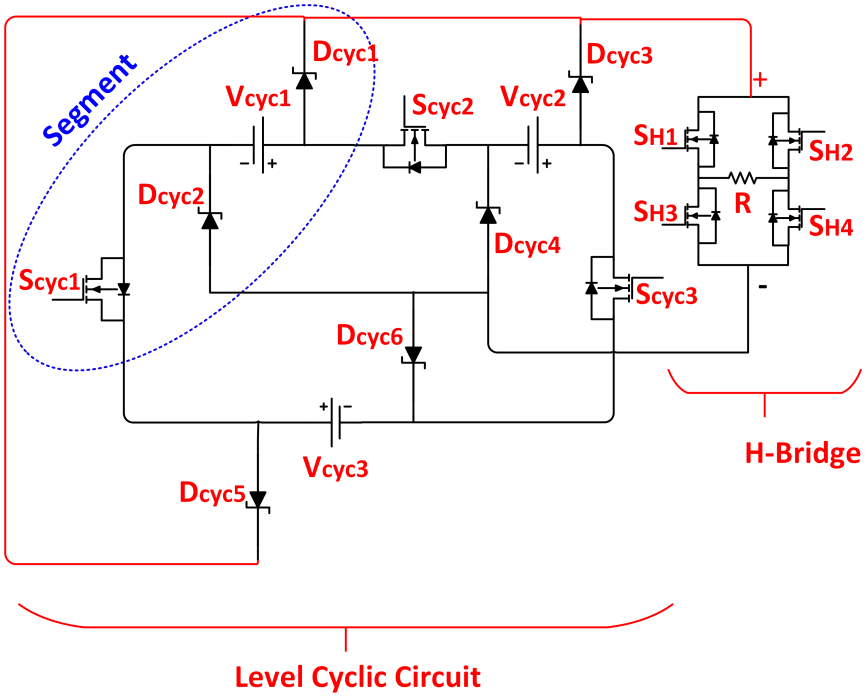

Figure 4.15: The basic structure of 7-level cyclic selection inverter

The number of output voltage levels of the proposed inverter in Figure 4.15 is seven with three sources only. It is worth noting that each voltage level apart from 0 V level is either produced by a series or parallel or series and parallel combination of the DC sources to realize the cyclic technique. This topology features an ease of extension by increasing the number of segments (Z_{cyc}) in the level cyclic circuit and cascading them. A straightforward generalization of the number of voltage levels (L_{cyc}) including zero with respect to the number of segments can be expressed as:

$$L_{cyc} = 2Z_{cyc} + 1 \tag{4.26}$$

It is worth mentioning that the total number of required power switches in the proposed inverter is seven as shown in the basic structure of Figure 4.15, where three switches ($S_{cyc_1}, S_{cyc_2}, S_{cyc_3}$) are used in the level cyclic circuit and the remaining four switches ($S_{H_1}, S_{H_2}, S_{H_3}, S_{H_4}$) are used in the H-bridge part. Additionally, the number of required diodes in this topology is exactly twice the number of sources. For instance, 6 diodes are required for 7-level structure while 10 diodes are required for 11-level structure. Additionally, all the diodes in the proposed topology are initially forward biased when the MOSFET switches are all off. The modes of operation of this inverter are detailed in the next section.

The proposed multilevel inverter here overcomes the redundancy in the DC sources and thus ensures they are evenly utilized. The proposed topology in this chapter removes the need for magmatic-core materials by selecting series and parallel combination of photovoltaic cells. The cyclic inverter has exactly the same performance as conventional pure sine-wave inverter with less circuit complexity. In addition, the cyclic structure features on-panel battery provision such that a complete generation and storage module is realized.

This topology generates the maximum available voltage unlike Golomb-sparse-Wichmann topology discussed in section 4.2.3. To generate 31 levels with the cyclic selection technique, 15 MOSFET switches are required in the level cyclic circuit while only 10 switches are required in the 5^{th} order modular Golomb-sparse-Wichmann ruler to generate the 29 level. The latter topology does not however generate the maximum voltage due the short circuit and also the DC sources are unevenly utilized. The effective number of MOSFETs in the 31-level cyclic selection inverter is approximately 5 (see section 4.4.3 for details).

4.3.2 Control Switching Strategy

The proposed inverter follows a simple but non-trivial direct conversion on and off methodology. This indicates that at any instant the controlled switching devices are either turned on or off at a low frequency to synthesize near sinusoidal 50 Hz waveform. In looking at the definition of X_{mn} in equation (4.2), it may be noted that the number of sources X_{mn} is 3 and *cyc* is realized only when n_{sub} is 2 sources. However, *cyc* is zero when n_{sub} is 0, 1 and 3 sources.

The proposed inverter can operate in seven different modes, where each one represents one voltage output level (Denoting the output voltage as $V_{out-cyc}$), both positive and negative modes of operation as shown in Figure 4.16. The proposed design here is capable of producing the following levels:

$$+(V_{cyc_1} + V_{cyc_2} + V_{cyc_3})$$

$$[+(V_{cyc_1} + V_{cyc_2}),+(V_{cyc_2} + V_{cyc_3}),+(V_{cyc_1} + V_{cyc_3})]$$

$$+(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$$

$$0$$

$$-(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$$

$$[-(V_{cyc_1} + V_{cyc_2}),-(V_{cyc_2} + V_{cyc_3}),-(V_{cyc_1} + V_{cyc_3})]$$

$$-(V_{cyc_1} + V_{cyc_2} + V_{cyc_3})$$

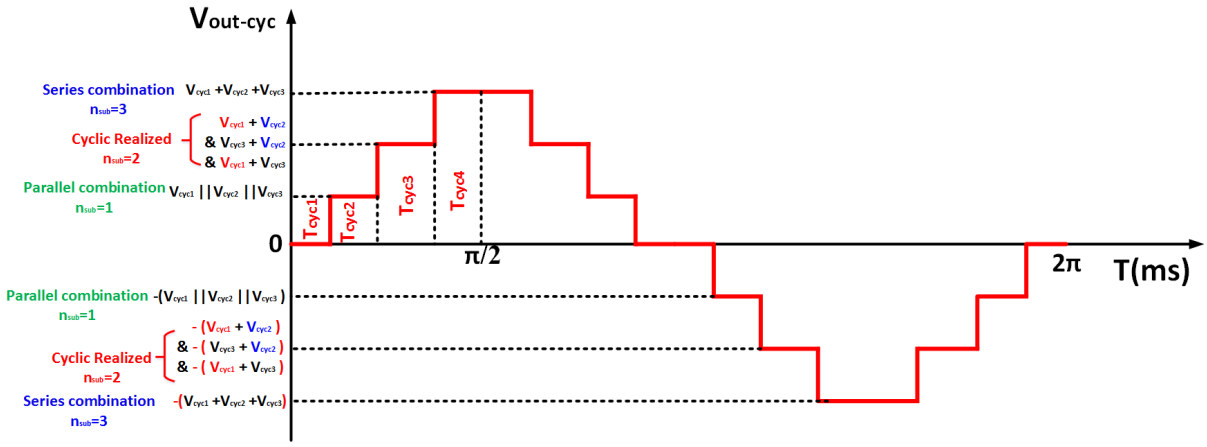

Figure 4.16: The proposed 7-level output voltage waveform of the cyclic selection inverter

Every two identical positive and negative voltage output levels correspond to a particular (n_{sub}). The output voltage levels of +($V_{cyc_1}||V_{cyc_2}||V_{cyc_3}$) and -($V_{cyc_1}||V_{cyc_2}||V_{cyc_3}$) correspond to $n_{sub} = 1$ while voltage levels of [+(V_{cyc_1}+V_{cyc_2})&+(V_{cyc_2}+V_{cyc_3})&+(V_{cyc_1}+ V_{cyc_3})], and -($V_{cyc_1} + V_{cyc_2}$)&-($V_{cyc_2} + V_{cyc_3}$)&-($V_{cyc_1} + V_{cyc_3}$)], correspond to $n_{sub} = 2$. The output levels at $n_{sub} = 3$ are the maximum voltage in the positive half cycle and minimum voltage in the negative half cycle. However, $n_{sub} = 0$ indicates that no voltage is selected and thus a zero level is produced at the load terminals at this instance.

The first level appears in Figure 4.16 across the load terminal R has a zero voltage 0 V at $n_{sub} = 0$. This level is selected by switching off all the MOSFET switches for T_{cyc1} time duration while the diodes in the level cyclic circuit are forward biased with no current flows through the load due to the fact that the drain source voltages of the top MOSFET switches are equal as shown in Figure 4.17. In addition, the second positive voltage level is selected at $n_{sub} = 1$ and is produced by switching

on S_{H_1} and S_{H_4} for T_{cyc2} duration while the other MOSFET switches are in non conducting state. The three DC sources in the cyclic circuitry appear in this case as a parallel combination due to the fact that all the diodes switches are forward biased as depicted in Figure 4.18. It is worth noting that the first and second levels are produced with no requirement for the cyclic techniques as the cells are evenly utilized. The third positive level, however, is selected at $n_{sub} = 2$ by shuffling the DC sources as illustrated in Table 4.8. The table shows that each two series connected DC sources are loaded for one third of T_{cyc_3} duration to synthesize the third level and thus they are evenly utilized. In other words, each DC source is loaded twice during T_{cyc_3} time duration by switching on only one MOSFET switch in one of the segments along with S_{H_1} and S_{H_4} while switches S_{H_2} and S_{H_3} are both off as shown in Figure 4.20, Figure 4.22 and Figure 4.24.

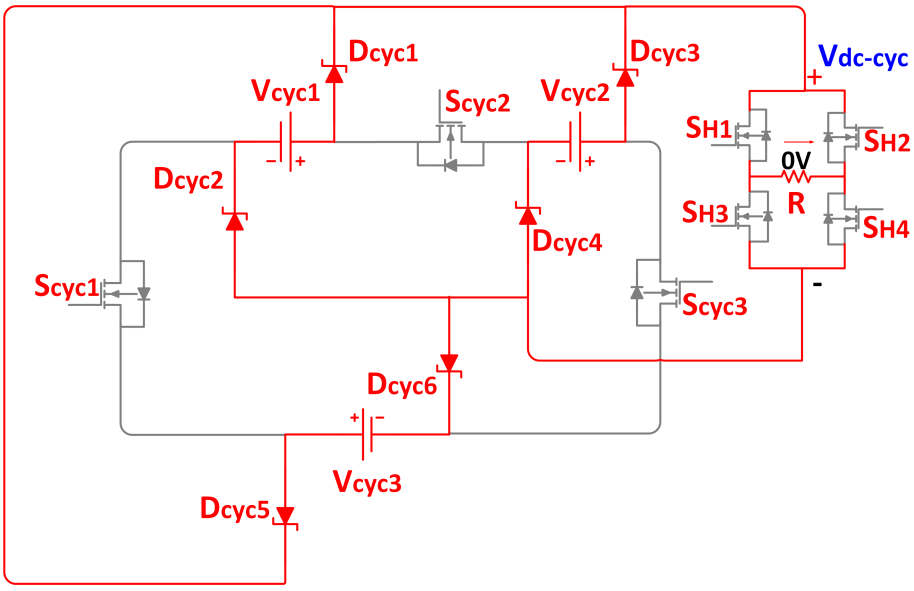

Figure 4.17: Mode of operation when $n_{sub} = 0 (V_{out-cyc} = 0)$

Table 4.8: $X_{mn} = 3$ & $n_{sub} = 2$ and $V_{out-cyc} = \pm 2V_{dc-cyc}$

V_{cyc_1}	V_{cyc_2}	V_{cyc_3}
1	1	0
1	2	1
2	2	2

Table 4.8 can be translated into a series combination of the DC sources as follows:

$$S_{mn} \begin{cases} (1,1,0) \Rightarrow V_{cyc_1} + V_{cyc_2} \\ (1,2,1) \Rightarrow V_{cyc_2} + V_{cyc_3} \\ (2,2,2) \Rightarrow V_{cyc_1} + V_{cyc_3} \end{cases}$$

$$\left.\begin{array}{l} (1,2,1) \Rightarrow V_{cyc_2} + V_{cyc_3} \\ (2,2,2) \Rightarrow V_{cyc_1} + V_{cyc_3} \end{array}\right\} cyc$$

Switches S_{cyc_2}, S_{H_1} and S_{H_4} are all on while the rest of the switches are off for one third of T_{cyc3} duration, connecting the two sources of V_{cyc_1} and V_{cyc_2} in series as shown in Figure 4.20 where the voltage across the load terminal R is $V_{out-cyc} = V_{cyc_1} + V_{cyc_2}$. This indicates that sources V_{cyc_1} and V_{cyc_2} are utilized for the first instant $(1,1,0)$ to generate the positive third level output across the load terminal for $\frac{1}{3}T_{cyc3}$ while V_{cyc_3} is not loaded at this instance. Further, Switches S_{cyc_3}, S_{H_1} and S_{H_4} are all on for one third of the duration T_{cyc3}, connecting the sources V_{cyc_2} and V_{cyc_3} in series while V_{cyc_1} is not loaded at this instance as shown in Figure 4.22. Lastly, switching on S_{cyc_1}, S_{H_1} and S_{H_4} while the rest of the switches are all off for one third of T_{cyc3} duration, resulting in series connection between the sources V_{cyc_1} and V_{cyc_3} with $V_{out-cyc} = V_{cyc_1} + V_{cyc_3}$ output voltage as shown in Figure 4.24. One may argue that the PV panels are not completely utilized, however, when the cells are not loaded,

they are charging the batteries. For example, V_{cyc_3} at the first instance is not loaded for $\frac{1}{3}T_{cyc3}$ time duration but it is charging its battery to ensure a complete panel utilization.

The fourth positive level is generated by switching any two MOSFET switches in the level cyclic circuit along with S_{H_1} and S_{H_4}; the output voltage across the load terminal is a series connection of the three sources $V_{out-cyc} = V_{cyc_1} + V_{cyc_2} + V_{cyc_3}$ as shown in Figure 4.26. It is worth mentioning that the only difference between the switching states in the positive half cycle and that in the negative half cycle is the H-bridge combinations. In the positive half cycle, the switches (S_{H_1} and S_{H_4}) are both switched on while the switches (S_{H_2} and S_{H_3}) are both switched off. The latter procedure of the H-bridge switches is, however, reversed during the negative half cycle as shown in Figures 4.19, 4.21, 4.23, 4.25 and 4.27.

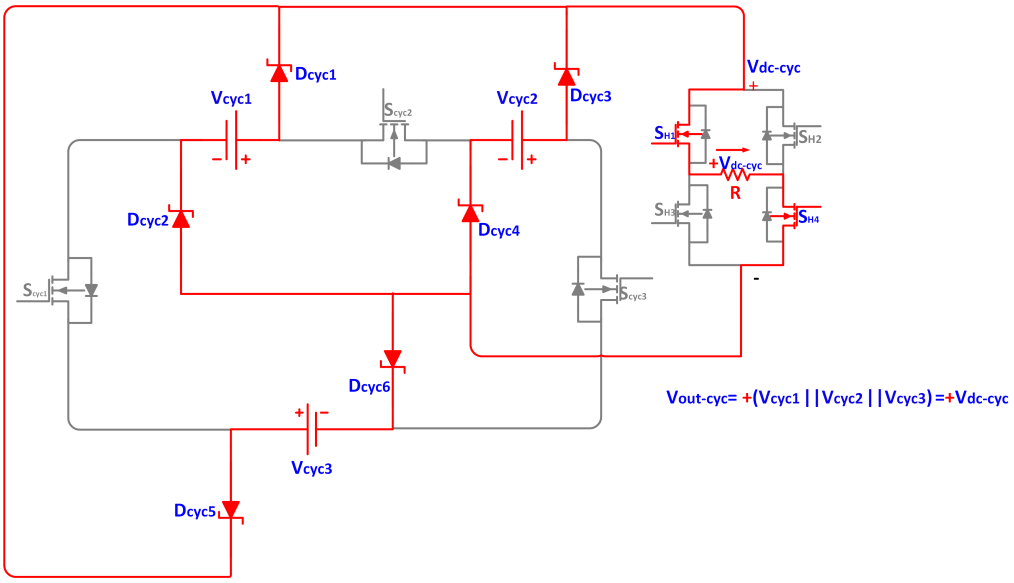

Figure 4.18: Mode of operation when $n_{sub} = 1$, $V_{out-cyc} = +(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$

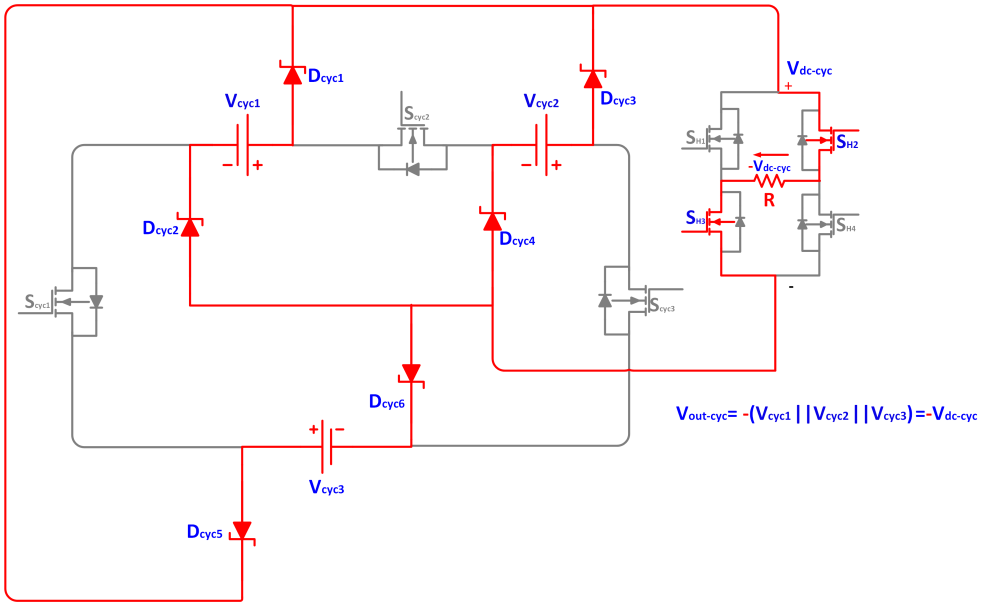

Figure 4.19: Mode of operation when $n_{sub} = 1$, $V_{out-cyc} = -(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$

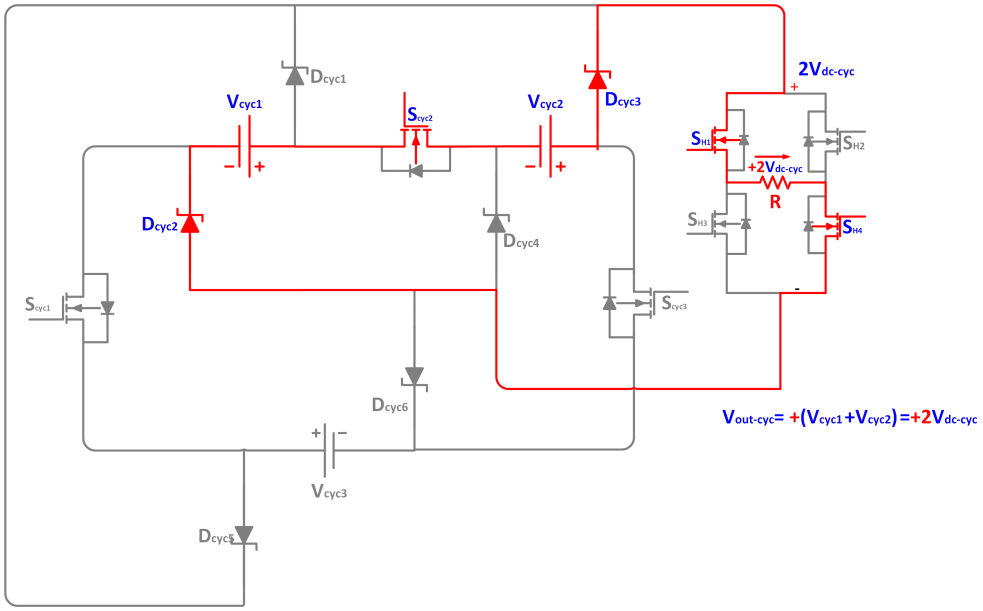

Figure 4.20: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = +(V_{cyc_1} + V_{cyc_2})$

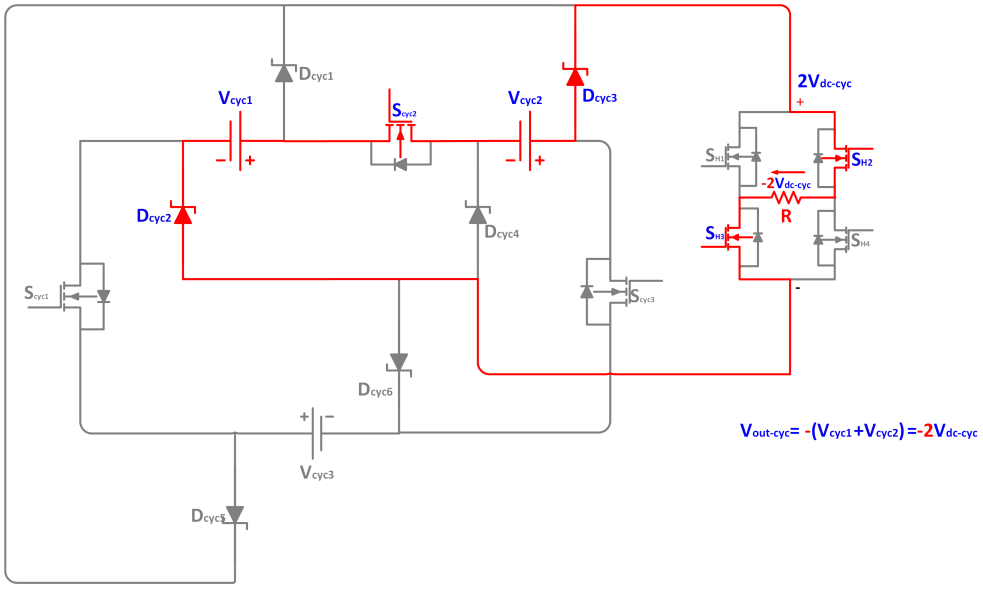

Figure 4.21: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = -(V_{cyc_1} + V_{cyc_2})$

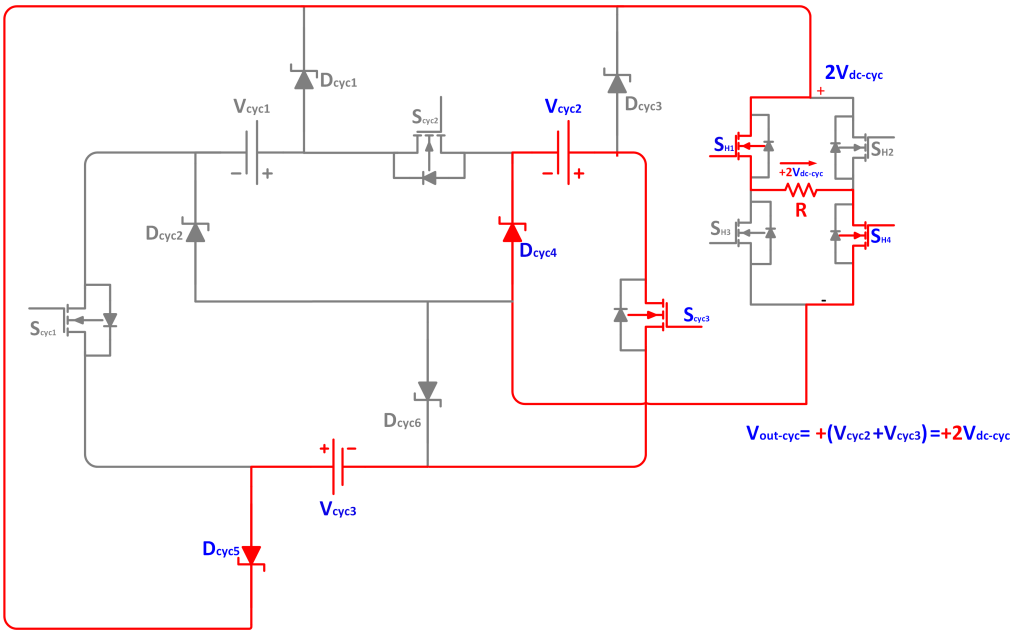

Figure 4.22: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = +(V_{cyc_2} + V_{cyc_3})$

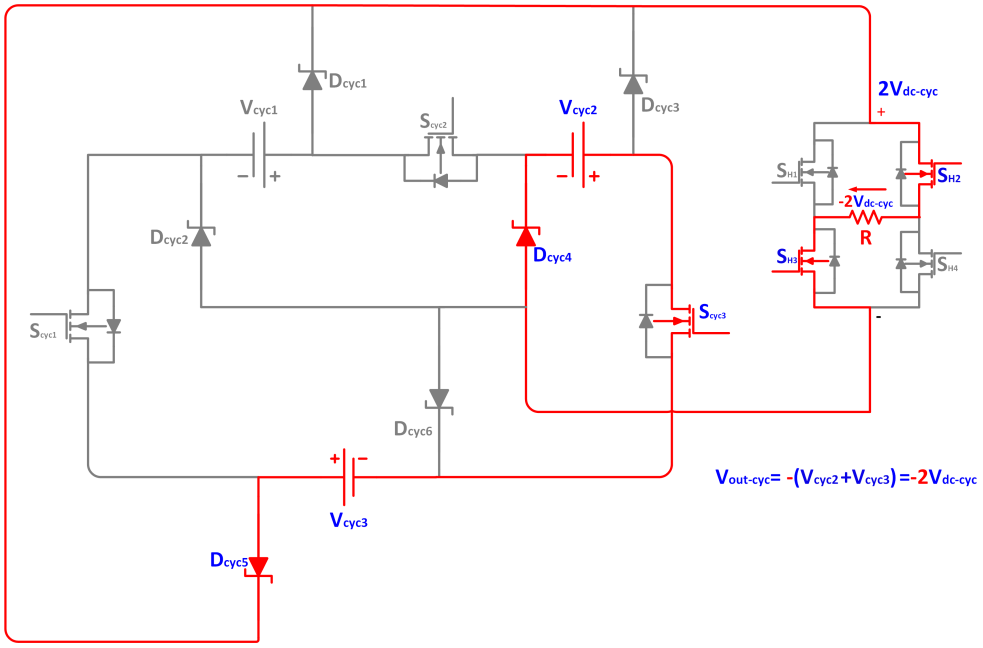

Figure 4.23: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = -(V_{cyc_2} + V_{cyc_3})$

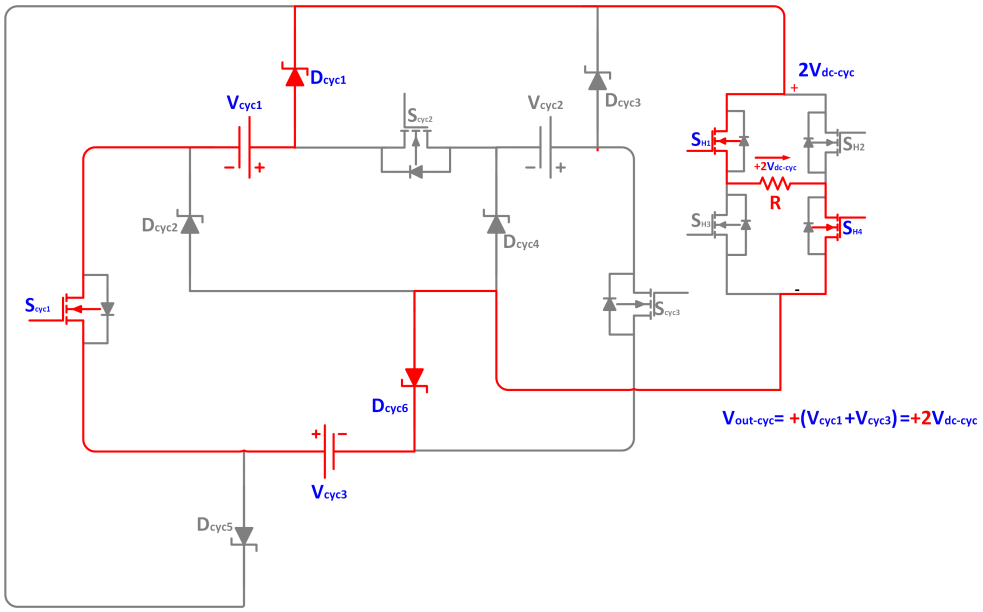

Figure 4.24: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = +(V_{cyc_1} + V_{cyc_3})$

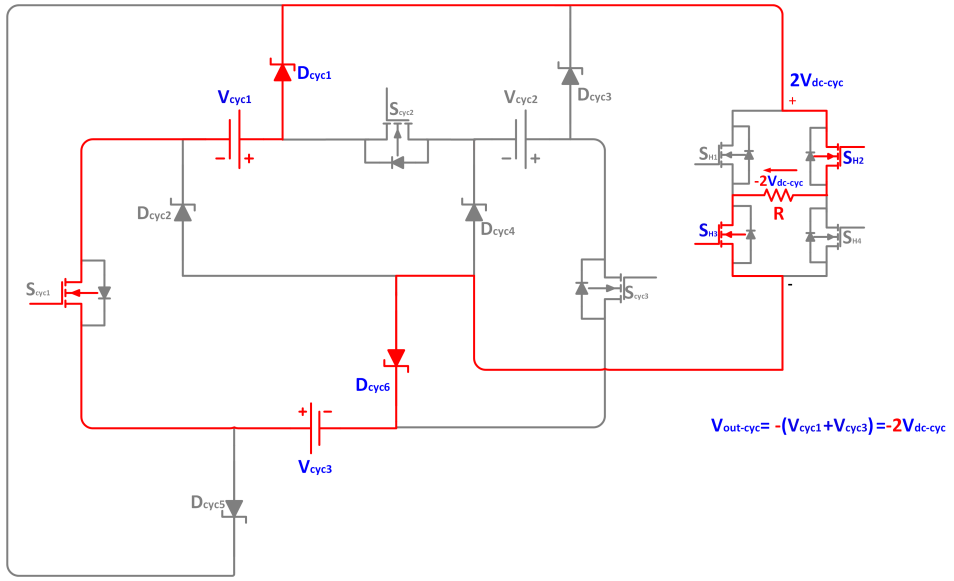

Figure 4.25: Mode of operation when $n_{sub} = 2$, $V_{out-cyc} = -(V_{cyc_1} + V_{cyc_3})$

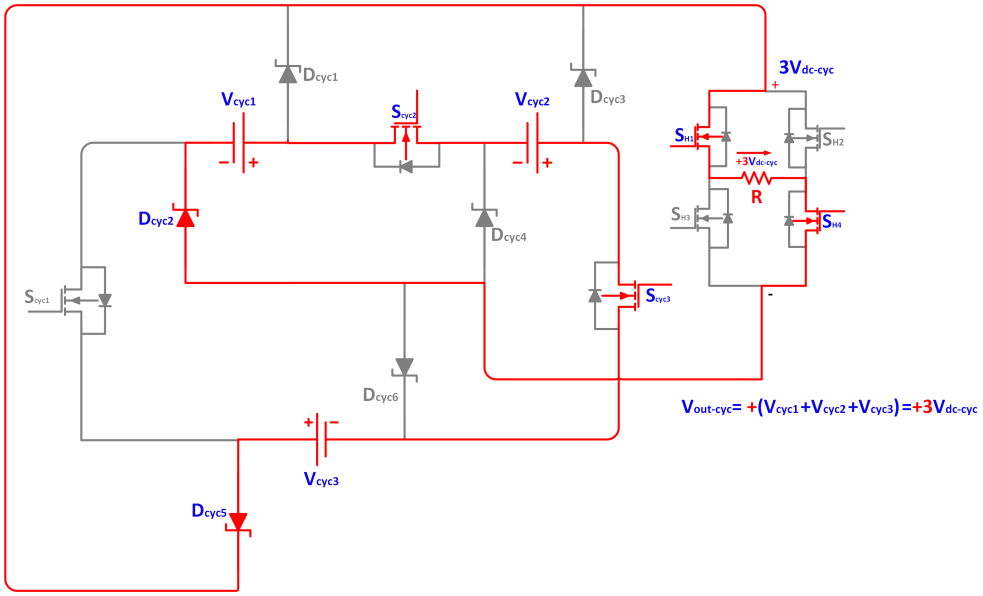

Figure 4.26: Mode of operation when $n_{sub} = 3$, $V_{out-cyc} = +(V_{cyc_1} + V_{cyc_2} + V_{cyc_3})$

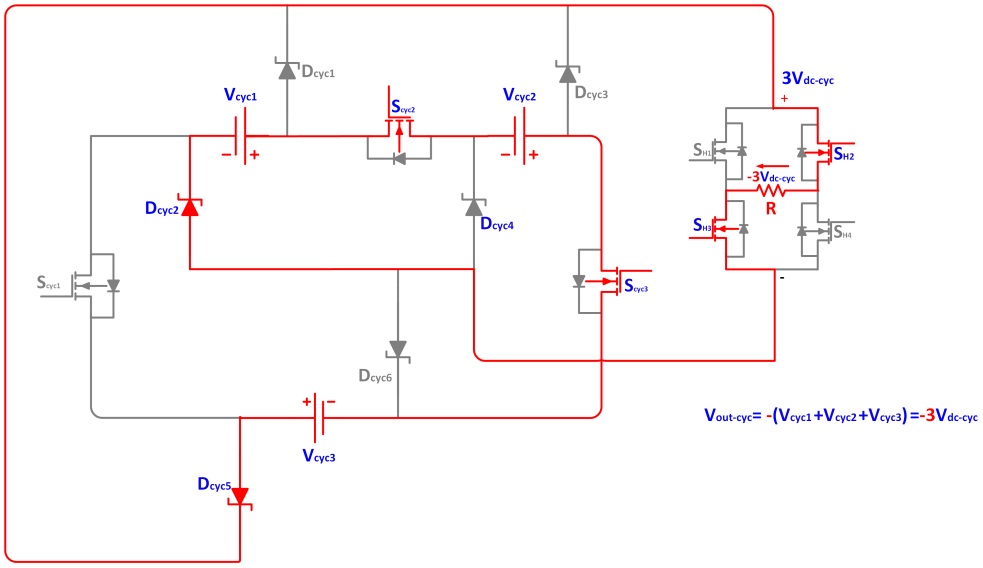

Figure 4.27: Mode of operation when $n_{sub} = 3$,$V_{out-cyc}$ = -($V_{cyc_1} + V_{cyc_2} + V_{cyc_3}$)

The switching states for the positive and negative half cycles are detailed in Table 4.9 and Table 4.10 respectively.

Table 4.9: Switching states for seven levels cyclic selection inverter of the positive half cycle

S_{cyc_1}	S_{cyc_2}	S_{cyc_3}	S_{H_1}	S_{H_2}	S_{H_3}	S_{H_4}	$V_{out-cyc}$	duration
0	0	0	0	0	0	0	0V	T_{cyc_1}
0	0	0	1	0	0	1	$+(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$	T_{cyc_2}
0	1	0	1	0	0	1	$+(V_{cyc_1} + V_{cyc_2})$	$1/3(T_{cyc_3})$
0	0	1	1	0	0	1	$+(V_{cyc_2} + V_{cyc_3})$	$1/3(T_{cyc_3})$
1	0	0	1	0	0	1	$+(V_{cyc_1} + V_{cyc_3})$	$1/3(T_{cyc_3})$
0	1	1	1	0	0	1	$+(V_{cyc_1} + V_{cyc_2} + V_{cyc_3})$	$2(T_{cyc_4})$
1	0	0	1	0	0	1	$+(V_{cyc_1} + V_{cyc_3})$	$1/3(T_{cyc_3})$
0	0	1	1	0	0	1	$+(V_{cyc_2} + V_{cyc_3})$	$1/3(T_{cyc_3})$
0	1	0	1	0	0	1	$+(V_{cyc_1} + V_{cyc_2})$	$1/3(T_{cyc_3})$
0	0	0	1	0	0	1	$+(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$	T_{cyc_2}
0	0	0	0	0	0	0	0V	T_{cyc_1}

Table 4.10: Switching states for seven levels cyclic selection inverter of the negative half cycle

S_{cyc_1}	S_{cyc_2}	S_{cyc_3}	S_{H_1}	S_{H_2}	S_{H_3}	S_{H_4}	$V_{out-cyc}$	duration
0	0	0	0	0	0	0	0V	T_{cyc_1}
0	0	0	0	1	1	0	$-(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$	T_{cyc_2}
0	1	0	0	1	1	0	$-(V_{cyc_1}+V_{cyc_2})$	$1/3(T_{cyc_3})$
0	0	1	0	1	1	0	$-(V_{cyc_2}+V_{cyc_3})$	$1/3(T_{cyc_3})$
1	0	0	0	1	1	0	$-(V_{cyc_1}+V_{cyc_3})$	$1/3(T_{cyc_3})$
0	1	1	0	1	1	0	$-(V_{cyc_1}+V_{cyc_2}+V_{cyc_3})$	$2(T_{cyc_4})$
1	0	0	0	1	1	0	$-(V_{cyc_1}+V_{cyc_3})$	$1/3(T_{cyc_3})$
0	0	1	0	1	1	0	$-(V_{cyc_2}+V_{cyc_3})$	$1/3(T_{cyc_3})$
0	1	0	0	1	1	0	$-(V_{cyc_1}+V_{cyc_2})$	$1/3(T_{cyc_3})$
0	0	0	0	1	1	0	$-(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$	T_{cyc_2}
0	0	0	0	0	0	0	0V	T_{cyc_1}

The functionality of each diode in the level cyclic circuit is illustrated in Table 4.11. For instance, the diodes in the level cyclic circuit are all ON when both output levels ($0V$,$+(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$ and $-(V_{cyc_1}||V_{cyc_2}||V_{cyc_3})$) are generated. However, only two diodes are ON when the output levels ($+(V_{cyc_1}+V_{cyc_2})$, $-(V_{cyc_1}+V_{cyc_2})$,$+(V_{cyc_2}+V_{cyc_3})$ $-(V_{cyc_2}+V_{cyc_3})$, $+(V_{cyc_1}+V_{cyc_3})$, $-(V_{cyc_1}+V_{cyc_3})$, $+(V_{cyc_1}+V_{cyc_2}+V_{cyc_3})$ and $-(V_{cyc_1}+V_{cyc_2}+V_{cyc_3})$) are produced. Diodes D_{cyc_1} and D_{cyc_6} are ON when $+(V_{cyc_1}+V_{cyc_3})$ and $-(V_{cyc_1}+V_{cyc_3})$ are generated while diodes D_{cyc_4} and D_{cyc_5} are conducting when the output levels $+(V_{cyc_2}+V_{cyc_3})$ and $-(V_{cyc_2}+V_{cyc_3})$ are produced.

Table 4.11: The functions of the diodes in the level cyclic segments

D_{cyc_1}	D_{cyc_2}	D_{cyc_3}	D_{cyc_4}	D_{cyc_5}	D_{cyc_6}	$V_{out-cyc}$
ON	ON	ON	ON	ON	ON	0 V
ON	ON	ON	ON	ON	ON	$+(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$ $-(V_{cyc_1}\|\|V_{cyc_2}\|\|V_{cyc_3})$
OFF	ON	ON	OFF	OFF	OFF	$+(V_{cyc_1}+V_{cyc_2})$ $-(V_{cyc_1}+V_{cyc_2})$
OFF	OFF	OFF	ON	ON	OFF	$+(V_{cyc_2}+V_{cyc_3})$ $-(V_{cyc_2}+V_{cyc_3})$
ON	OFF	OFF	OFF	OFF	ON	$+(V_{cyc_1}+V_{cyc_3})$ $-(V_{cyc_1}+V_{cyc_3})$
OFF	ON	OFF	OFF	ON	OFF	$+(V_{cyc_1}+V_{cyc_2}+V_{cyc_3})$ $-(V_{cyc_1}+V_{cyc_2}+V_{cyc_3})$

The overall switching frequency of the proposed inverter in this chapter is given by Equation (4.27).

$$f_{sw} = S_{cycSeg} . f_{fundamental} \tag{4.27}$$

Where: $f_{fundamental}$ is the fundamental frequency (50 Hz) of the output signal of the proposed inverter here, S_{cycSeg} is the number of segments in the output waveform shown in Figure 4.16 in one complete cycle 0 to 2π. The timing steps of the cyclic selection inverter $T_{cyc_1}, T_{cyc_2}, T_{cyc_3}$ are determined using a new mathematical method of known amplitude which is discussed in detail in Chapter 5. The timing steps determination of the new method is based on a mean square error voltage regression approach to minimize the lower order harmonic components in the output signal.

4.4 Performance of Cyclic Selection Inverter

4.4.1 PWM Inverter and Cyclic Selection Inverter Comparisons

One may question why should not a conventional PWM inverter with a string of PV panels be used instead of the direct conversion cyclic selection system. Having a string of PV panels connected to an ordinary PWM inverter ensures even source utilization and generates a pure sinusoidal waveform. The conventional PWM inverter has been widely criticised due to its circuit complexity, EMI and switching losses. Viable solutions that have less circuit complexity and maximum efficiency should be put up. Here, it is proved mathematically that the cyclic selection staircase direct conversion system has exactly the same performance as a conventional core-based PWM inverter (pure sine-wave output).

Assuming a lossless PWM inverter which generates a voltage and current for a load with output power coming from the input source. The basic power flow in a PWM inverter using a string of series solar panels with storage (capacitors or batteries) as an input is shown in Figure 4.28.

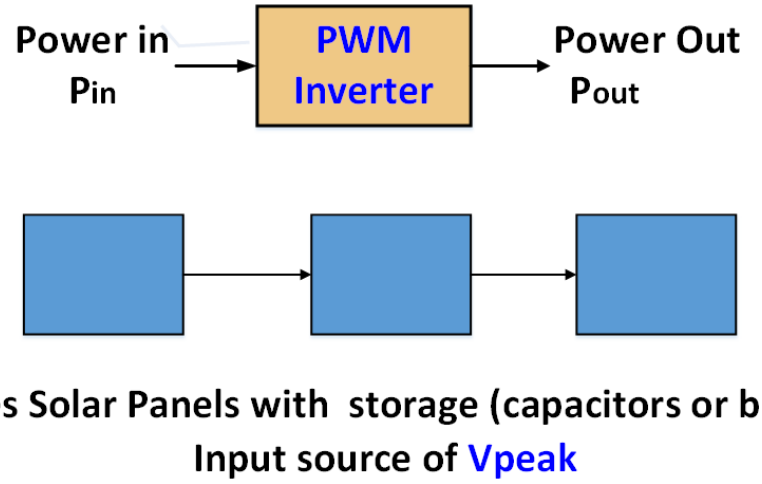

Figure 4.28: Basic power flow from series solar panels with batteries in a PWM inverter

Thus,

$$P_{in} = P_{out} \tag{4.28}$$

where P_{in} and P_{out} are the input power and output power of a conventional inverter, respectively.

If the instantaneous power of a sinusoid is given by (4.29):

$$P(t) = 2P_{avg}(\sin(\omega t))^2 \tag{4.29}$$

where $P(t)$ is the instantaneous power of a sinusoidal waveform, P_{avg} is the average power of sine-wave signal which can be expressed as $P_{peak} = 2P_{avg}$. P_{peak} is the peak power of a sine-wave signal.

The instantaneous input current $I_{in}(t)$ is given by:

$$\begin{aligned} I_{in}(t) &= \frac{P(t)}{V_{peak}} \\ &= \frac{2P_{avg}(\sin(\omega t))^2}{V_{peak}} \end{aligned} \tag{4.30}$$

where V_{peak} is the peak voltage of a sine-wave signal.

The integration of the periodic sinusoidal waveform defined in equation (4.30) for the positive half cycle from 0 to π is expressed as:

$$\begin{aligned} Area &= \int_0^{\pi} \frac{2P_{avg}(\sin(\omega t))^2}{V_{peak}} dt \\ &= \frac{\pi P_{avg}}{V_{peak}} \end{aligned} \tag{4.31}$$

Note that $\frac{\pi P_{avg}}{V_{peak}}$ is the area under the squared sine-wave half cycle and thus the average current (assuming capacitive sources) of a half cycle can be obtained by integrating the squared sinusoidal waveform over a half cycle (0 to π) and then dividing by a half period π as in equation (4.32).

$$\begin{aligned} I_{avg} &= \frac{1}{\pi} \int_0^{\pi} \frac{2P_{avg}(\sin(\omega t))^2}{V_{peak}} dt \\ &= \frac{P_{avg}}{V_{peak}} \end{aligned} \tag{4.32}$$

Equation (4.32) shows that the average current contribution of each solar panel with storage (capacitor or battery) to the sinusoidal output of the conventional inverter is defined as the average power over the peak voltage.

Now considering the battery or capacitor array panels connected to a cyclic direct conversion system as an assumption. The instantaneous current per segment in this

case is given by:

$$\begin{aligned} I(t) &= I_{peak}\sin(\omega t) \\ &= \frac{2P_{avg}\sin(\omega t)}{V_{peak}} \end{aligned} \tag{4.33}$$

It is mentioned in the previous section that the cyclic design system ensures an even panel utilization by selecting series and parallel combinations of the cells to generate a good quality sine-wave. It is worth noting that the number of parallel cells varies asymptotically by $\frac{1}{\sin(\omega t)}$ while the number of series cells varies by $\sin(\omega t)$. The number of parallel cells contribute to the multilevel output waveform varies by $\frac{1}{\sin(\omega t)}$ as the number of levels increases. The average current per segment is therefore expressed by:

$$\begin{aligned} I_{avg} &= \frac{1}{\pi}\frac{2P_{avg}}{V_{peak}}\int_0^{\pi}(\sin(\omega t))^2 dt \\ &= \frac{P_{avg}}{V_{peak}} \end{aligned} \tag{4.34}$$

Equation (4.34) gives the same answer as equation (4.32) and this indicates the cyclic technique where the cells are selected in series and parallel combinations has exactly the same performance as the conventional PWM inverter of series input panels with storage (capacitors or batteries).

4.4.2 Power Switching Losses for a Finite Segments in Cyclic Level Circuit

Switching a single MOSFET by a PWM technique that has a resistive load at each transition (off to on and vice versa) causes power losses. Denoting the maximum voltage through the load from the source by V_p. The current through the MOSFET is maximum, I_p, during on state while it is 0 A during off state. In contract, the voltage across the MOSFET is maximum, V_p, during off state while it is 0 V during on state. The instantaneous current and voltage during the transition t_{full} can be expressed in equation (4.35) and equation (4.36) respectively.

$$I(t) = I_p(1 - \frac{t}{t_{full}}) \tag{4.35}$$

$$V(t) = V_p(\frac{t}{t_{full}}) \tag{4.36}$$

Thus, the instantaneous average power loss can be written as:

$$P_{avg}(t) = V_p.I_p.(\frac{t}{t_{full}}).(1 - \frac{t}{t_{full}}) \tag{4.37}$$

The dissipated energy per transition can be obtained by integrating the average power from (0 to t_{full}) as equated in (4.38).

$$\begin{aligned} E_{mos} &= V_p.I_p.\int_0^{t_{full}} (\frac{t}{t_{full}} - \frac{t^2}{t_{full}^2})dt \\ &= \frac{V_p.I_p.t_{full}}{6} \end{aligned} \tag{4.38}$$

Assuming the transition time (t_{rise}) from off state to on state is equal to (t_{full}) and thus the total energy dissipated due to on and off states is given by:

$$\begin{aligned} E_{mos} &= \frac{V_p.I_p.(t_{full} + t_{rise})}{6} \\ &= \frac{V_p.I_p.T_{sw_{tran}}}{3} \end{aligned} \tag{4.39}$$

Noting that $T_{sw_{tran}}$ is the overall transition time $T_{sw_{tran}} = t_{full} + t_{rise}$. The total average power dissipation in a single switch is presented in equation (4.40)

$$P_{avgTot} = \frac{V_p.I_p.T_{sw_{tran}}.f_{sw}}{3} \tag{4.40}$$

L_{cyc} is given in equation (4.26) as the total number of output voltage levels (positive and negative) including zero in the cyclic inverter. Denoting the number of non zero voltages in the positive or negative half cycle as L_{half} which equals the number of segments Z_{cyc}. It is worth noting that the number of MOSFET switches in the level cyclic circuit is equal to the number of segments. Thus, the power loss in each MOSFET switch in the level cyclic circuit is given by:

$$P_{lossswitch} = \frac{\frac{V_p}{L_{half}}.I_p.T_{sw_{tran}}.f_{sw}}{3} \tag{4.41}$$

Denoting the number of MOSFETs in the segments of the level cyclic circuit by N_{mos} and hence equation (4.41) can be rewritten as:

$$P_{lossswitch} = \frac{\frac{V_p}{N_{mos}}.I_p.T_{sw_{tran}}.f_{sw}}{3} \tag{4.42}$$

4.4.3 The Effective and Optimum Number of MOSFET Switches in the Segments

One may wonder whether there is an effective number of MOSFET switches in designing the level cyclic circuit as the number of levels increases. The question to be also asked whether there is an optimum (minimum) number of MOSFET switches for a given maximum voltage and current of PV panels. It seems that the answer to the questions lies in the power dissipation due to MOSFET ON resistance and the PWM switching transition losses. It is true that the number of levels of the cyclic inverter increases by increasing the number of segments Z_{cyc} in the level cyclic circuit. The beauty of the cyclic technique in terms of the switching operation is the fact that the current does not flow through the MOSFET switches when the sources are in parallel as previously shown in Figures 4.18, and 4.19, and thus additionally no conduction losses occur at this stage. There is however a full load current flowing through all the MOSFETs except one when the maximum voltage level is generated as shown in Figure 4.26 and Figure 4.27. The conduction losses due to the ON resistance for one MOSFET switch is given by equation (4.43).

$$P_{avg} = (I_{rms})^2.R_{ds(on)} \tag{4.43}$$

Note that $R_{ds(on)}$ is the ON resistance of the selected MOSFET, I_{rms} is the root mean square (rms) current through the MOSFET. Giving the equation of the instantaneous current per segment in (4.33), equation (4.43) can be rewritten as:

$$P_{avg}(t) = (I_{peak})^2.(\sin(\omega t))^2.R_{ds(on)} \tag{4.44}$$

For a number of MOSFET switches N_{mos} in the level cyclic circuit equation (4.44) can be expressed as:

$$P_{avg}(t) = N_{mos}(I_{peak})^2.(\sin(\omega t))^2.R_{ds(on)} \tag{4.45}$$

The number of MOSFET switches in series in the level cyclic circuit varies as $\sin(\omega t)$ and thus additionally the series current and MOSFET ON resistance vary as $\sin(\omega t)$. However, the number of MOSFETs in parallel varies as $\frac{1}{\sin(\omega t)}$ as the voltage and the current get smaller and thus in turn the MOSFET ON resistance gets smaller by $\frac{1}{\sin(\omega t)}$.

Thus,

$$P_{avg}(t) = N_{mos}(I_{peak})^2.(\sin(\omega t))^2.\frac{R_{ds(on)}.(\sin(\omega t))}{\frac{1}{(\sin(\omega t))}} \tag{4.46}$$

The average power dissipation can be obtained by integrating the fourth power of a sinusoidal waveform over a half cycle (0 to π) and dividing by a half period π as in equation (4.47).

$$\begin{aligned} P_{avg} &= \frac{1}{\pi} N_{mos}(I_{peak})^2.R_{ds(on)} \int_0^{\pi} (\sin(\omega t))^4 dt \\ &= \frac{3}{8} N_{mos}(I_{peak})^2.R_{ds(on)} \end{aligned} \tag{4.47}$$

It is worth noting that the number of switched MOSFETs at maximum output voltage in the level cyclic circuit is $(N_{mos} - 1)$ for N_{mos} segments. Switching N_{mos} MOSFETs full count causes a short circuit. Therefore, the power dissipation due to MOSFET ON resistance in equation (4.47) can be written as:

$$P_{avg} = \frac{3}{8}(N_{mos} - 1)(I_{peak})^2.R_{ds(on)} \tag{4.48}$$

Where $\frac{3}{8}(N_{mos}-1)$ is the effective number of MOSFETs in the level cyclic circuit. It can be argued that a level cyclic circuit with 16 MOSFETs as an example is very complex and has huge power dissipation. The effective number of MOSFETs is, however, 6. This numerical example shows a substantial reduction in the power dissipation.

The total power dissipation P in the series MOSFETs in the level cyclic circuit is obtained by adding both equations (4.48) and (4.42) as:

$$\begin{aligned} P &= P_{avg} + P_{lossswitch} \\ &= \frac{3}{8}(N_{mos}-1)(I_{peak})^2.R_{ds(on)} + \frac{\frac{V_p}{N_{mos}}.I_p.T_{sw_{tran}}.f_{sw}}{3} \end{aligned} \tag{4.49}$$

Finally, equation (4.49) is differentiated with respect to N_{mos} and set to zero to obtain the optimum number of MOSFETs in the level cyclic circuit as follows:

$$\begin{aligned} \frac{dP}{dN_{mos}} &= \frac{3}{8}(I_{peak})^2.R_{ds(on)} - \frac{V_p.I_p.T_{sw_{tran}}.f_{sw}}{3.N_{mos}^2} \\ &= 0 \end{aligned} \tag{4.50}$$

Thus,

$$N_{mos} = \frac{\sqrt{\frac{8.V_p.T_{sw_{tran}}.f_{sw}}{I_p.R_{ds(on)}}}}{3} \tag{4.51}$$

Taking $V_p = 345$ V, $I_p = 6.1$ A, $T_{sw_{tran}} = 100$ ns, $R_{ds(on)} = 0.011\Omega$ and switching this at high frequency $f_{sw} = 50$ kHz for example to obtain N_{mos}. Thus, the total number of MOSFETs in the level cyclic circuit is $N_{mos} = 5$ and the overall power dissipation in equation (4.49) is approximately $P = 1.2$ W. The effective number of MOSFET switches in the segments is 2. This numerical example gives a 99.9% efficiency of the use of the proposed cyclic selection technique.

Comparing this effect at a low switching frequency ($f_{sw} = 5$ kHz as an example) with the same assumptions as previous. Hence, $N_{mos} = 2$ and the overall power dissipation is approximately 0.32 W. One may argue that the cyclic selection is optimized only at low frequencies in which the switching losses in the circuit is reduced to minimum. However, switching at low frequencies increases the size of the electromagnetic materials.

4.5 Experimental Implementation

4.5.1 Single - Phase, Seven - Level Cyclic Selection Inverter Overall Layout

The laboratory implementation layout for the single-phase seven-level cyclic selection multilevel inverter is shown below in Figure 4.29. The major components of the setup are two dual USB rechargeable solar powered batteries (GRDE ®Ultrathin 10000 mAh Solar Power Bank, 5V-550 mAh Monocrystalline silicon solar panel, Polymer Lithium ion battery USBs (5V & 1A and 5V & 2.1 A) and four Schottky diodes of 500 mV forward voltage (DIODES INC. B340A-13-F SCHOTTKY Rectifier, Single, 40V, 3A) and six MOSFET switches (FAIRCHILD SEMICONDUCTOR, FQP30N06, N-CHANNEL MOSFET, 60V, 32A, TO-220) (two in the cyclic circuit, four in the H-Bridge part). The type of diode used here is suitable for low voltage applications and has low power loss and high efficiency. Mbed NXP LPC1768 microcontroller is used here to control the MOSFET switches through four DigitalOut pins (Pin_{21},

Pin_{22}, Pin_{23}, Pin_{24}) via an on-line C++ compiler. The Mbed microcontroller is powered through a USB cable using a PC. There is a control circuit between the main MOSFET switches and the microcontroller pins and this includes: one PV MOSFET driver of four pins (OPTOISOLATOR, 4.5KV VOM1271TCT-ND) and one (TO-220) MOSFET switch and one 180 Ω resistor). The major components in this setup: MOSFET switches and their control circuits, Schottky diodes and Mbed microcontroller are mounted on a printed circuit board PCB which is designed using PROTEUS PCB design software. The MOSFET driver used in this application has a logic compatible input and obtains all the required current to drive its internal circuit from the LED current on the low voltage side of the isolator barrier. This saves the space and cost of providing external power supplies.

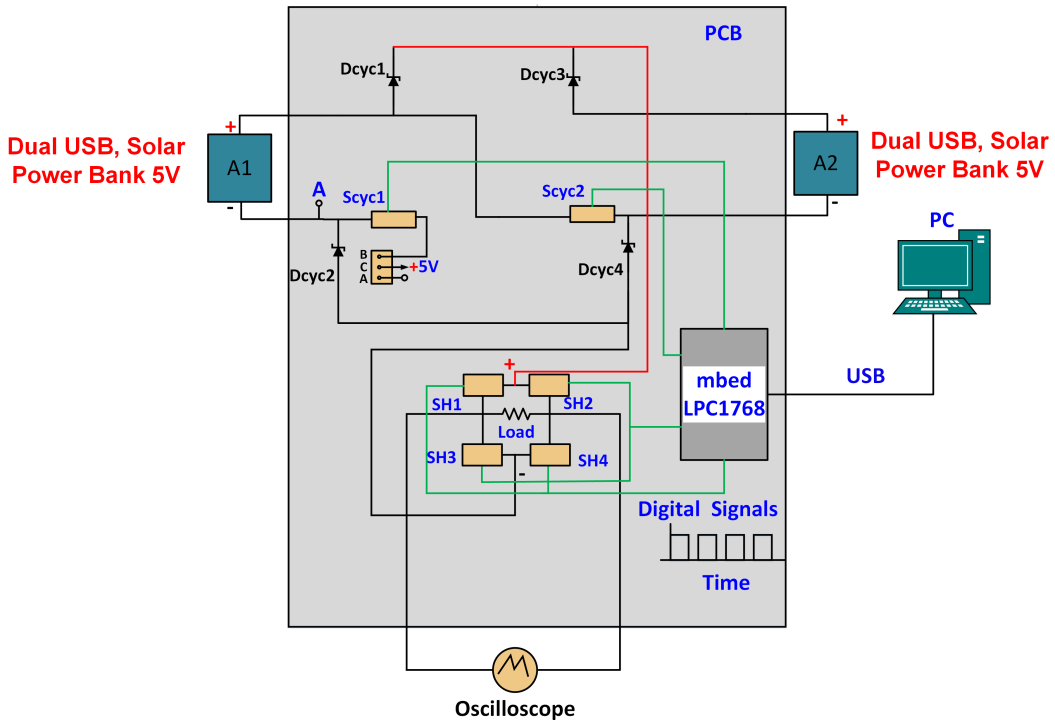

Figure 4.29: Implementation of the seven-level cyclic selection inverter

Here, the microcontroller sets the states of the MOSFET according to the switching control scheme explained in section 4.3.2 to synthesize a multilevel waveform. At any instant, each individual DigitalOut pin (Pin_{21} to Pin_{24}) is set either to zero to turn it off, or to one to turn it on to form the switching control signals for a complete period 2π. Each signal goes to Pin_1 of each photovoltaic drivers to turn it on or turn it off and thus in turn sets the MOSFET switches in the H-bridge and the cyclic circuits off or on with respect to the switching states in section 4.3.2. For example, the signal generated at Pin_{21} goes to Pin_1 of the MOSFET driver to turn it on or off according to the switching scheme discussed previously and this in turn turns on or off S_{cyc1}. The time duration of each individual control signal is set in the main program. It is worth mentioning that the method of determining the timing steps here will be discussed in detail in the next chapter. The desired output multilevel waveform is captured at the load terminals through two oscilloscope probes in differential mode and the switching control scheme is automated in C++ code (Appendix A).

The overall pin configuration of the proposed inverter is shown in Figure 4.30.

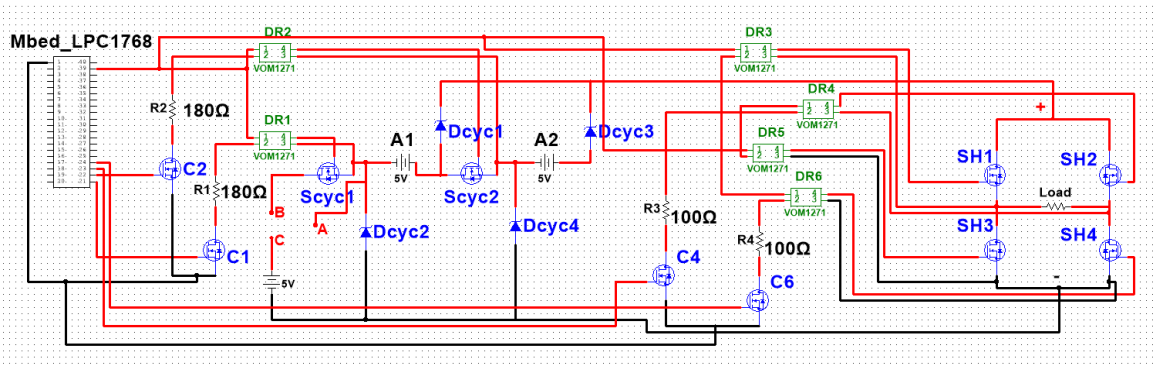

Figure 4.30: The design circuit of the seven-level cyclic selection multilevel inverter

The internal circuit of the photovoltaic driver includes an LED element which appears

across Pin_1 and Pin_2 while a photovoltaic cell and a rapid turn off circuitry appears across Pin_3 and Pin_4.

In Figure 4.30, Pin_1 of DR_1, DR_2, DR_3 and DR_5 is connected to VU Pin (5V) of the Mbed. Pin_2 of DR_1 and DR_2 is connected to a limiting current resistance of 180 Ω value and TO-220 N-channel MOSFET switch to prevent the LED from burning up and then grounded in the Mbed side. The MOSFET switches in the driving circuit of DR_1 and DR_2 is controlled through the digital out pins of the Mbed Pin_{21} and Pin_{22} respectively. Also, Pin_2 of DR_3 is connected to Pin_1 of DR_6 while Pin_2 of DR_5 is connected to Pin_1 DR_4. Pin_2 of DR_4 and DR_6 is connected to a limiting current resistance of 100 Ω value and TO-220 N-channel MOSFET switch and then grounded in the Mbed side. The MOSFET switches in the driving circuit of DR_4 and DR_6 are controlled through the digital out pins of the Mbed Pin_{23} and Pin_{24} respectively. Pin_4 of DR_1, DR_2, DR_3, DR_4, DR_5 and DR_6 is connected to the gate of S_{cyc_1}, S_{cyc_2}, S_{H_1}, S_{H_3}, S_{H_2} and S_{cyc_2} respectively. In contrast, Pin_3 of DR_1, DR_2, DR_3, DR_4, DR_5 and DR_6 is connected to the source of S_{cyc_1}, S_{cyc_2}, S_{H_1}, S_{H_3}, S_{H_2} and S_{cyc_2} respectively.

It can be seen from the design circuit that the positive terminal of the solar battery (A1) is connected to the anode of D_{cyc_1} while its negative terminal is connected to the cathode of D_{cyc_2}. Further, the positive terminal of the solar battery (A2) is connected to the anode of D_{cyc_3} while its negative terminal of the battery is connected to the cathode of D_{cyc_4}. The cathodes of D_{cyc_1} and D_{cyc_3} are connected together to form the positive terminal of the H-bridge circuit while the anodes of D_{cyc_2} and D_{cyc_4} form the negative terminal. The drain of S_{cyc_2} is connected to the anode of D_{cyc_1} while the source is connected to the cathode of D_{cyc_4}. The source of S_{cyc_1} is connected to the cathode of D_{cyc_2} while the drain is connected to a jumper of three connectors (B,C

and A). Connector C is connected to 5 V power supply for a testing purpose. (Note that the USB terminal used in this application is 5V & 2.1 A)

In the H-bridge circuit, S_{H_2} source is connected to S_{cyc_4} drain whereas S_{H_1} source is connected to S_{cyc_3} drain. S_{H_1} and S_{H_2} drains are connected together to form the positive terminal while S_{H_3} and S_{H_4} are connected together to form the negative terminal. The load terminals appear across S_{H_1} & S_{H_2} sources and S_{H_3} & S_{H_4} drains. (Note that each two MOSFETs in the H-bridge (S_{H_1} and S_{H_4}) and (S_{H_2} and S_{H_3}) are controlled using one driving circuit which will be detailed in the next section)

4.5.2 Component Characteristics and Design

4.5.2.1 Rechargeable Solar Powered Lithium Ion Battery

The battery pack used in this application consists of two main parts: a solar panel and a polymer lithium ion battery. This module can be charged by two different charging methods, either the mounted solar panel or a USB.

The current-voltage (I-V) and power-resistance (P-R) characteristic curves of the solar packs used here are investigated by practical measurements as shown in Figure 4.31 and Figure 4.32 respectively. These packs have a 10000 mAh capacity as specified by the manufacture which means that these batteries can deliver 3000 mA for three hours or 500 mA for 20 hours as shown in Figure 4.33. The greatest current produced by the battery is obtained under the short circuit conditions as given by the manufacture.

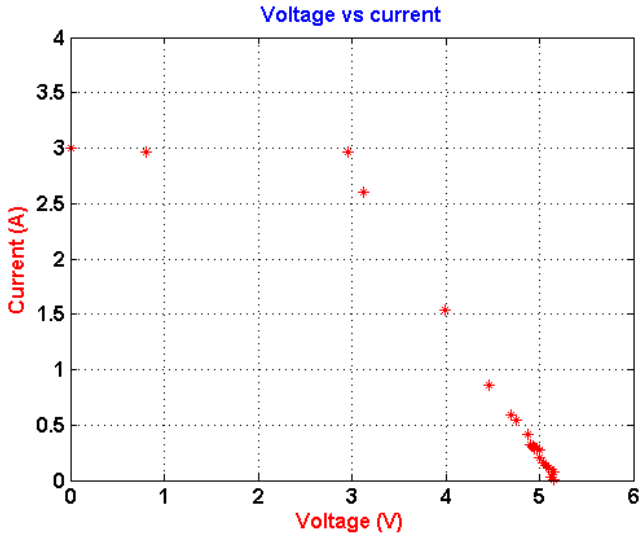

Figure 4.31: The I-V characteristics of the solar powered lithium ion battery pack

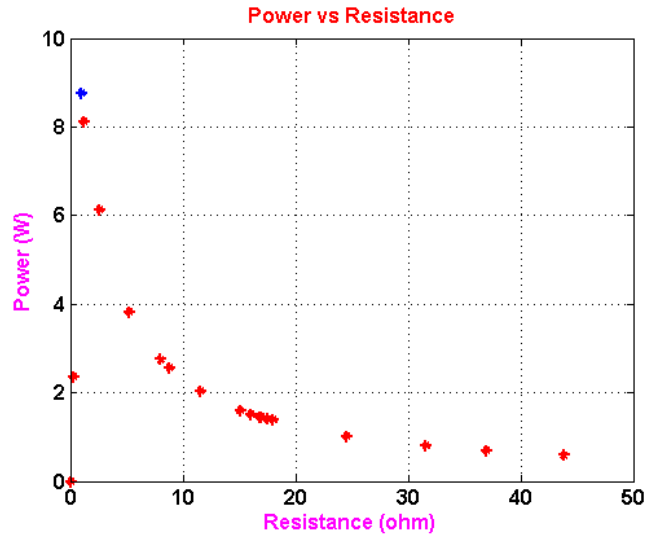

Figure 4.32: The P-R characteristics of solar powered lithium ion battery pack

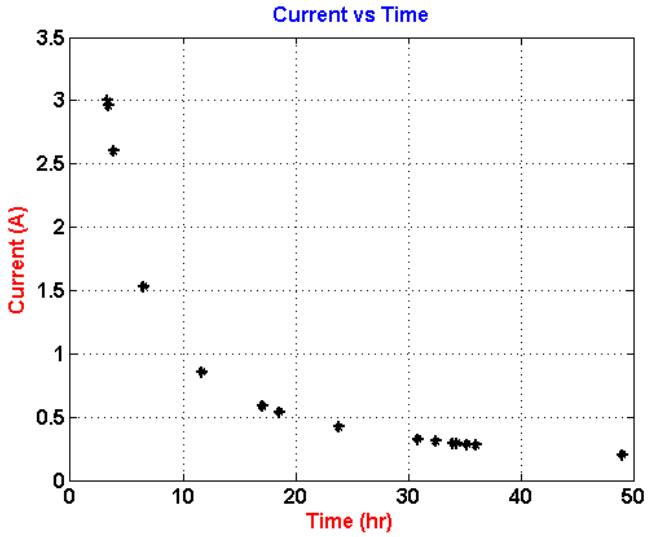

Figure 4.33: The current vs time of the solar powered lithium ion battery pack

It is deduced from Figure 4.31 that the I-V characteristic of the solar powered lithium ion battery pack has a similar curve to I-V characteristics of solar panels. In fact, this battery operates at a constant current (3 A) in the range between (0 V to 3 V). However, it operates as a current and a voltage source between the voltages range of 3 V and 5 V. The slope of the decade line of the battery in this range is 1.2 Ω^{-1}. Re-plotting the curve such that the voltage in the y-axis and the current in the x-axis resulting in 0.833 Ω slope in the voltage range of (3 V to 5 V).

The electrical performance of the battery pack used here is summarized in Table 4.12.

Table 4.12: Electrical performance of the solar powered lithium ion battery pack

Open circuit Voltage	5 V
Short Circuit Voltage	3 A
Optimum Load	1 Ω
Optimum Power	8.7 W

The most noticeable feature of Figure 4.33 is that the time increases as the required

current decreases. In other words, the battery delivers a small amount of current for a longer time period before it runs out of charge while it is capable to deliver a large amount of current upto 3 A for a shorter time period.

4.5.2.2 Photovoltaic MOSFET driver VOM1271

The photovoltaic MOSFET drivers are used in this application to drive the N-channel MOSFET switches of the cyclic inverter. An attempt of direct driving of the photovoltaic drivers from the microcontroller through the digital out pins with various limiting current resistors of 68 Ω, 32.8 Ω, and 0 Ω (short wire) values is made to draw different currents in the control circuit up to 40 mA maximum in the internal LED. The attempted tested circuit is designed to control an N-channel MOSFET which in turn switches on and off 5V power supply into 10kΩ load. The rise time, the fall time, frequency and the voltage waveform of the drain source of the photo driver in the test circuit are also investigated. This design however is unreliable as it causes a short circuit in the Mbed digital output pins. An alternative driving circuit is designed at which Pin_2 of the photo drivers DR_1, DR_2, DR_4, DR_6 are connected to a current limiting resistor and a N channel MOSFET switch to boost the current to the required 20 mA in the internal LED as shown in Figure 4.34 and Figure 4.35. This results in switching on and off to the main MOSFET switches S_{cyc_1}, S_{cyc_2}, S_{H_1}, S_{H_2}, S_{H_3} and S_{H_4} according to the switching strategy presented in section 4.3.2.

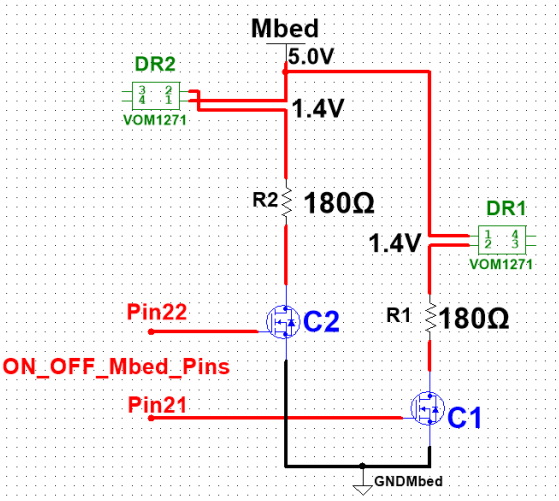

Figure 4.34: Control circuit of N-channel MOSFET switches in the level cyclic segments

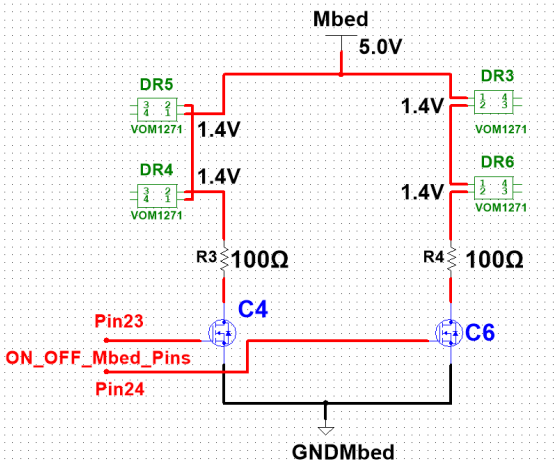

Figure 4.35: Control circuit of N-channel MOSFET switches in H-Bridge circuit

The value of the current limiting resistors in DR_1 and DR_2 circuits differs from those in DR_4 and DR_6 circuits for the reason that each pair of photo drivers in the H-Bridge circuit (DR_3 & DR_6) (DR_4 & DR_5) are connected in series. This denotes that double the LED forward voltage is considered in calculating the current limit resistance as shown in equation (4.52) unlike that in DR_1 and DR_2 circuit where only one LED

forward voltage is taken into account as equated in (4.53).

$$R_H = \frac{V_{Mbed_{5V}} - 2V_{LED_{forward}}}{I_{Level_{req}}} \tag{4.52}$$

Where: $V_{Mbed_{5V}}$ is the supply voltage from the Mbed pin 5V, $V_{LED_{forward}}$ is the forward voltage (1.4 V) of the internal LED of VOM1271 and $I_{Level_{req}}$ is the required current level in the control circuit 20 mA. Thus,

$$R_H = 100\Omega$$

$$Rc = \frac{V_{Mbed_{5V}} - V_{LED_{forward}}}{I_{Level_{req}}} \tag{4.53}$$

$$R_c = 180\Omega$$

4.6 Experimental and Simulation Results

4.6.1 Seven - Level, DC to AC Cyclic Selection Multilevel Inverter Simulation

The Simulink Simulation of the single-phase, 7-level, 50 Hz DC to AC, cyclic selection multilevel inverter is shown in Figure 4.36.

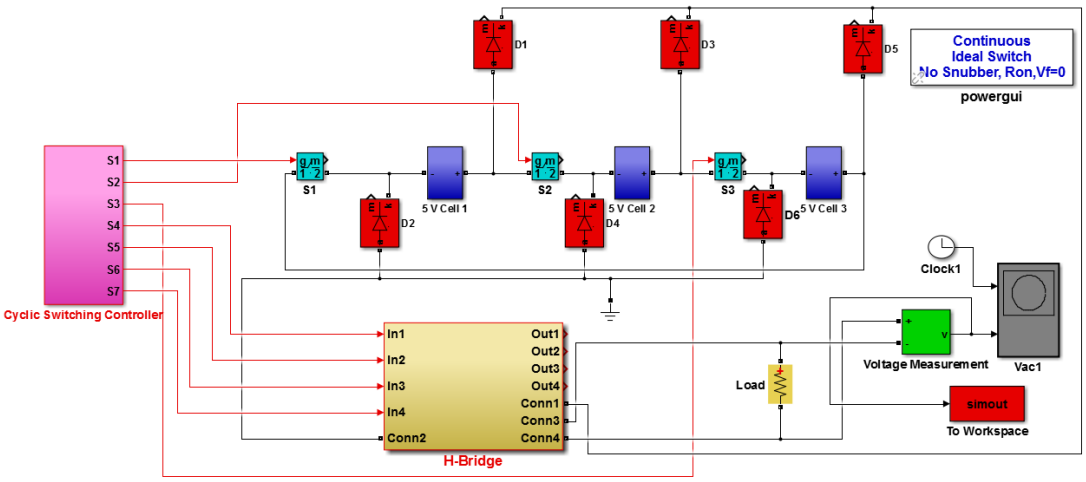

Figure 4.36: The simulation setup of the 7-level cyclic selection multilevel inverter

This figure shows the setup for 7-level, using a switching controller block which controls each MOSFET switch according to the switching states (Chapter 4 for details). The setup also shows three DC battery cells of 5V each are employed as an input source of the inverter. Three ideal switches are used in the cyclic circuit while four ideal switches are used in the H-bridge subsystem circuit to switch on and off the batteries according to the switching states. The subsystem design of the H-bridge circuit is depicted in Figure 4.37. The output waveform is captured across a resistive load of 5kΩ by a Simulink Scope which clocks at the current simulation time.

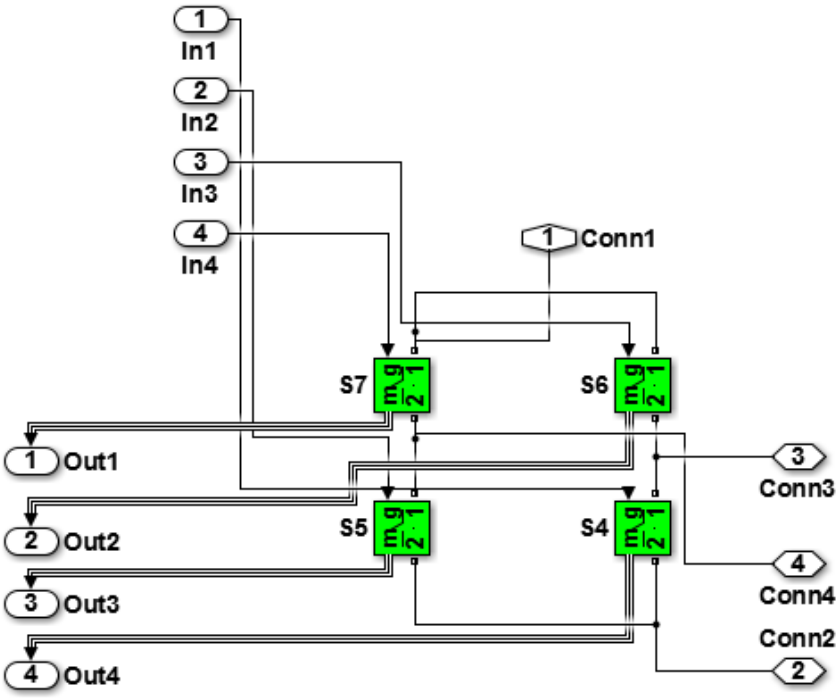

Figure 4.37: The Simulink layout of the H-bridge circuit

The controller block is implemented through the switching states table to form the switching pulses for both the positive and negative half cycles as shown in Figure 4.38.

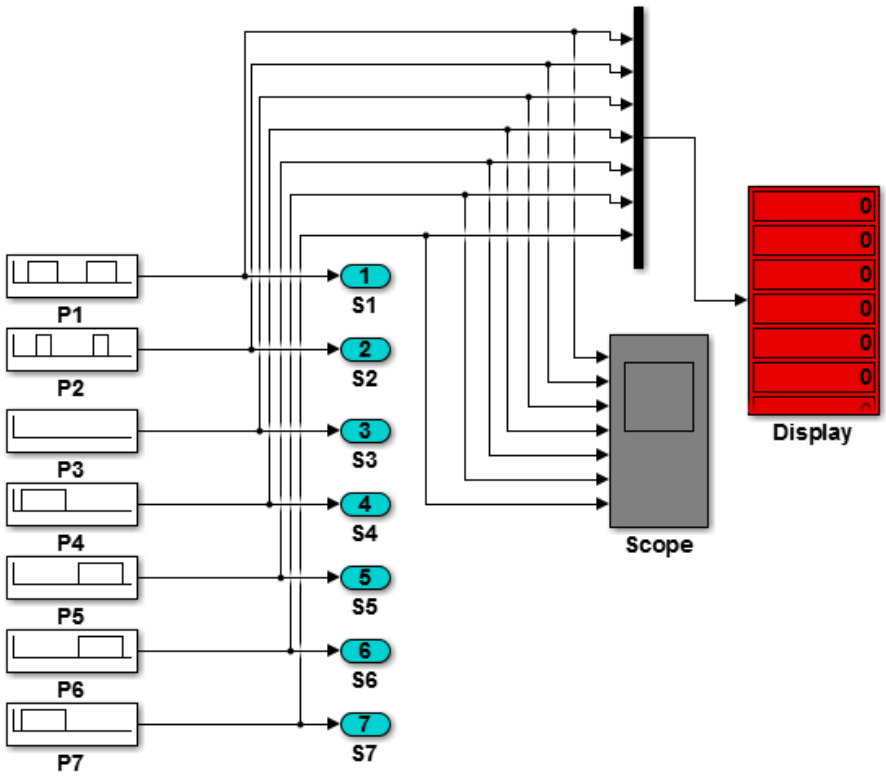

Figure 4.38: The Simulink layout of the cyclic selection switching controller

The controller consists of a repeating sequence stair masks that set the vector outputs of P1, P2, P3, P4, P5, P6 and P7 to the switching states each at a sample time of 0.625 ms. These vectors are captured by a display through a multiplex vector signals bar (Mux block) of 7 inputs. The vector signals are passed through the subsystem output ports (S1, S2, S3, S4, S5, S6 and P7) to the ideal switches to form the required staircase voltage output waveform. These vectors (switching pulses of S1, S2, S3, S4,

S5, S6 and S7 at each instant respectively) are represented in 7 arrays as:

[00100111100100000010011110010000]

[00010110011010000001011001101000]

[00001001111001000000100111100100]

[01111111111111100000000000000000]

[00000000000000000111111111111110]

[00000000000000000111111111111110]

[01111111111111100000000000000000]

The sampling time (0.625 ms) for each vector signal is obtained by dividing one complete cycle period (20 ms) by the number of values in the arrays. The waveform pulses of each ideal switch is illustrated in Figure 4.39. The evenly utilized DC sources are noticeable in the switching pulses waveforms. The cyclic is realized at $n_{sub} = 2$ in which only one MOSFET switch in the level cyclic circuit is conducting for one third of the time duration of the generated level as observed in the control waveforms.

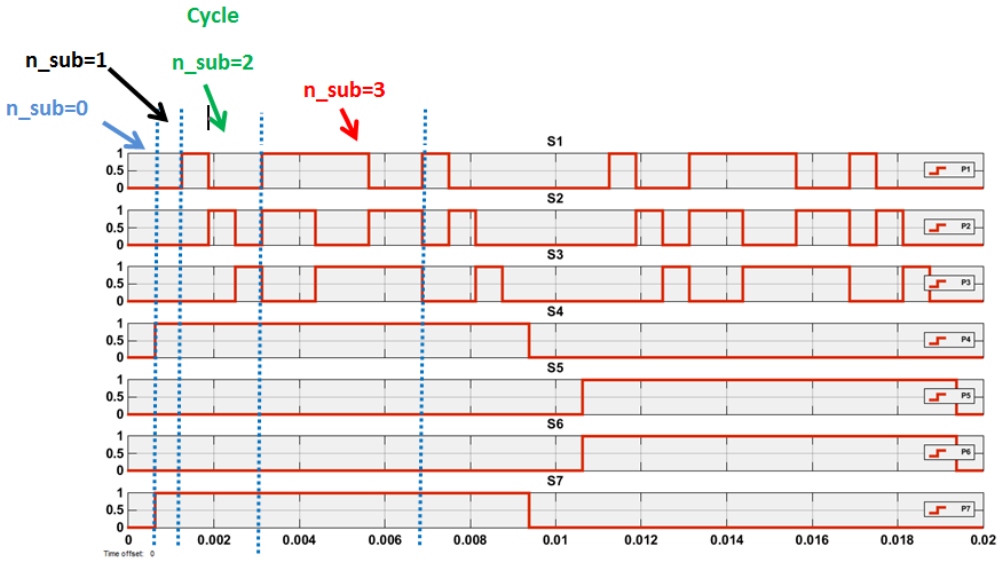

Figure 4.39: The output waveform pulses of the cyclic switching controller that are fed to ideal switches (One complete cycle)

In the switching states of the simulation results, we examined switching any two MOSFETs in the level cyclic circuit to generate the maximum voltage level as observable in the control waveforms at $n_{sub} = 3$. The output voltage waveform across the load and its fast Fourier transform FFT analysis for one complete cycle are captured through the powergui block and displayed in Figure 4.40.

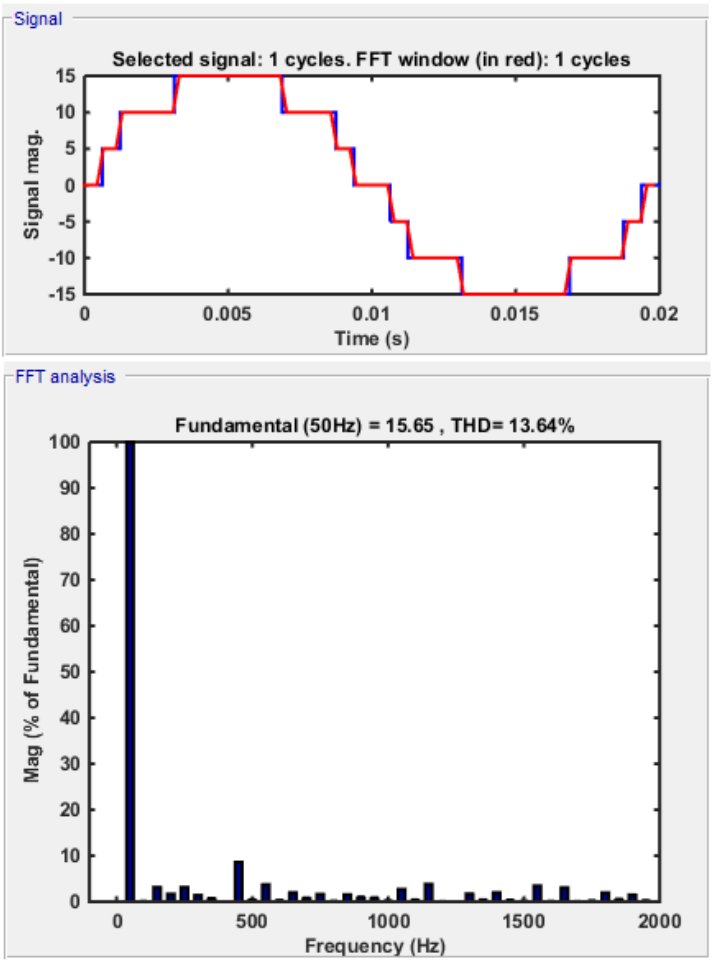

Figure 4.40: The 7-level cyclic selection, voltage output waveform and FFT analysis (adjusted time duration of the steps)

The peak voltage of the 50 Hz, seven-level cyclic selection inverter is 15 V which agrees well with the expected maximum voltage of the input sources. The THD of the voltage waveform is 13.64 % and the magnitude of the third harmonic component is 3.13% of the fundamental. It is not possible to set the time durations of the voltage steps to the optimized values (Chapter 5 for details) due to the limitations in the Simulink simulator. The time duration of the steps in this case was adjusted by using a heuristic technique based on repeating the switching states of the levels in the

vector arrays. A dramatic reduction in THD and the magnitude of 3^{th} component with respect to the fundamental was observed. The output waveform of the 7-level cyclic inverter and the FFT analysis for equally spaced time steps within a quarter cycle is displayed in Figure 4.41. The latter is included to analyze the reduction in the THD and the third harmonic component in the tuned time duration signal obtained in Figure 4.40.

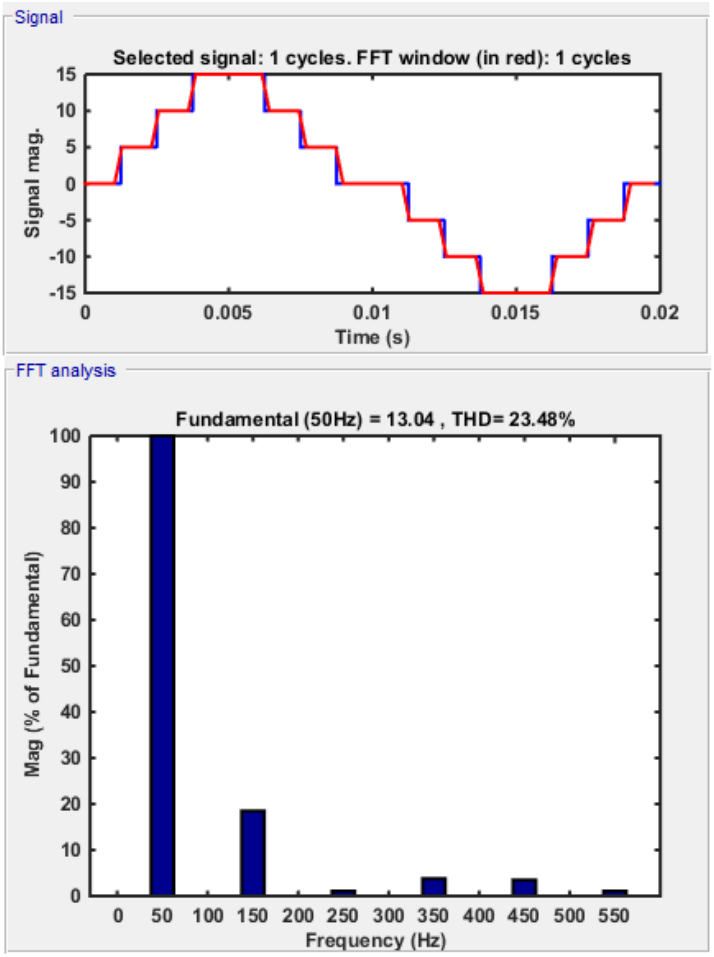

Figure 4.41: The 7-level cyclic selection voltage output waveform and FFT analysis for equally spaced time steps within a quarter cycle (0 to 5 ms)

It can be seen that the THD of the output waveform with adjusted time duration of

the steps are reduced by 9.84% (Figure 4.40) when compared to equally spaced steps waveform (Figure 4.41). Additionally, the third harmonic component is reduced to 3.13% compared to 19% in the equal steps quarter cycle waveform.

4.6.2 Seven - Level, DC to AC Cyclic Selection Multilevel Inverter Experimental Prototype

The implemented prototype of the 7-level, cyclic selection 50 Hz multilevel inverter is shown in Figure 4.42 and the complete experimental setup is discussed in section 4.5.1.

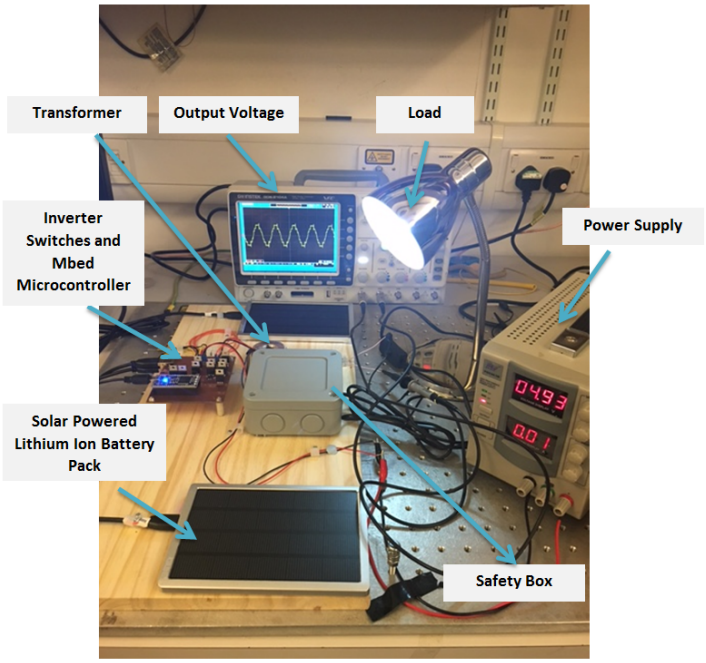

Figure 4.42: The experimental setup of the 7-level cyclic selection inverter

The circuit was initially tested with different resistive loads across the level cyclic

circuit terminals with the BC jumper on, with and without the power supply (5 V) to investigate the DC voltage levels as illustrated in Table 4.13.

Table 4.13: The output DC voltage levels of the level cyclic circuit at various loads

Battery A_1	Battery A_2	5V Supply (C)	Load	S_{cyc_1}	S_{cyc_2}	Output
ON	ON	OFF	30 ohm	OFF	OFF	4.5 V
ON	ON	OFF	30 ohm	ON	OFF	4.5 V
ON	ON	OFF	30 ohm	OFF	ON	9.18 V
ON	ON	OFF	85 ohm	OFF	OFF	4.633 V
ON	ON	OFF	85 ohm	ON	OFF	4.633 V
ON	ON	OFF	85 ohm	OFF	ON	9.51 V
ON	ON	OFF	225 ohm	OFF	OFF	4.7 V
ON	ON	OFF	225 ohm	ON	OFF	4.7 V
ON	ON	OFF	225 ohm	OFF	ON	9.72 V
ON	ON	ON	30 ohm	OFF	OFF	4.5 V
ON	ON	ON	30 ohm	ON	OFF	9.36 V
ON	ON	ON	30 ohm	OFF	ON	9.21 V
ON	ON	ON	30 ohm	ON	ON	14 V
ON	ON	ON	85 ohm	OFF	OFF	4.633 V
ON	ON	ON	85 ohm	ON	OFF	9.58 V
ON	ON	ON	85 ohm	OFF	ON	9.52 V
ON	ON	ON	85 ohm	ON	ON	14.59 V
ON	ON	ON	225 ohm	OFF	OFF	4.7 V
ON	ON	ON	225 ohm	ON	OFF	9.7 V
ON	ON	ON	225 ohm	OFF	ON	9.71 V
ON	ON	ON	225 ohm	ON	ON	14.76 V

It is seen from Table 4.13 that the two solar packed batteries A_1 and A_2 are in parallel at various loads when S_{cyc_1} and S_{cyc_2} are off. Switching S_{cyc_2} ON while S_{cyc_1} is OFF at 30 Ω load without the power supply (0 V), results in a series combination of the two battery packs with the output voltage level of 9.18 V. Switching S_{cyc_1} ON while S_{cyc_2} is OFF with the power supply (5 V) at 30 Ω load, results in a series combination of the power supply and the battery pack A_1 with the output voltage level of 9.36 V. These two controlling states show that the cyclic technique is realized by switching

ON only one MOSFET in the level cyclic circuit at which the output voltage is the series combination of the switched sources as shown in Table 4.13.

The C++ program code for a repeated full cycle (0 to 2π) (Code is included in Appendix A) is applied to the Mbed microcontroller via the on - line complier where the timing steps of the output waveform (quarter cycle representation: $T_{cyc_1} = 0.00052s$, $T_{cyc_2} = 0.00116s$, $T_{cyc_3} = 0.00148s$ and $T_{cyc_4} = 0.00184s$) are set with respect to the optimization theory (Chapter 5). It is worth noting that the calculation of the timing steps is based on the maximum available voltage that the inverter can generate at 1 kΩ load (13.59 V) in which A in equation 5.7 is chosen to be 13.59 V for minimum distortion. Furthermore, the inverter can generate the following voltage steps at 1 kΩ ($\alpha_0 = 0, \alpha_1 = 4.49V, \alpha_2 = 9.19V$ and $\alpha_3 = 13.59V$). Thus, using equation 5.7 for a quarter cycle representation, the switching angles of $\theta_0 = 0.052\pi$, $\theta_1 = 0.168\pi$ and $\theta_2 = 0.316\pi$ are obtained. The control pulses are generated according to the switching states of this inverter and passed through the microcontroller digital output pins to the photovoltaic drivers to control the MOSFETs. The code is designed such that any two consecutive time durations for the same output level is switched only once to avoid switching losses. For instance, the zero output level between the positive and negative half cycles is switched for double the time duration.

The output waveform shown in Figure 4.43 is captured using two scope probes in a differential mode to measure the voltage difference across 1 kΩ load that is placed at the H - bridge terminals.

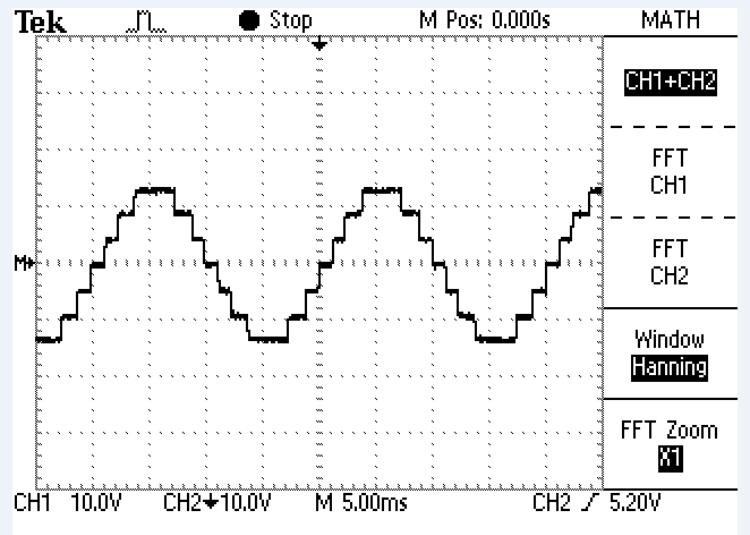

Figure 4.43: The AC staircase waveform output of the cyclic selection inverter (two scope probes in a differential mode) (Optimized timing steps)

A miniature toroidal transformer with dual secondary windings is hence used across the output terminals of the H-bridge to replace the resistive load for testing purposes as shown in the revised setup Figure 4.44. This allows a single scope probe to be used to capture the voltage output waveform and its FFT. A power resistive load of 1 kΩ is connected to one of the parallel secondary windings while the other winding is used to capture the voltage output waveform through a single scope probe. The primary winding is connected to a dimmable 3 W OMNI-LED desk lamp (85 - 240 ACV) through a cable safety box.

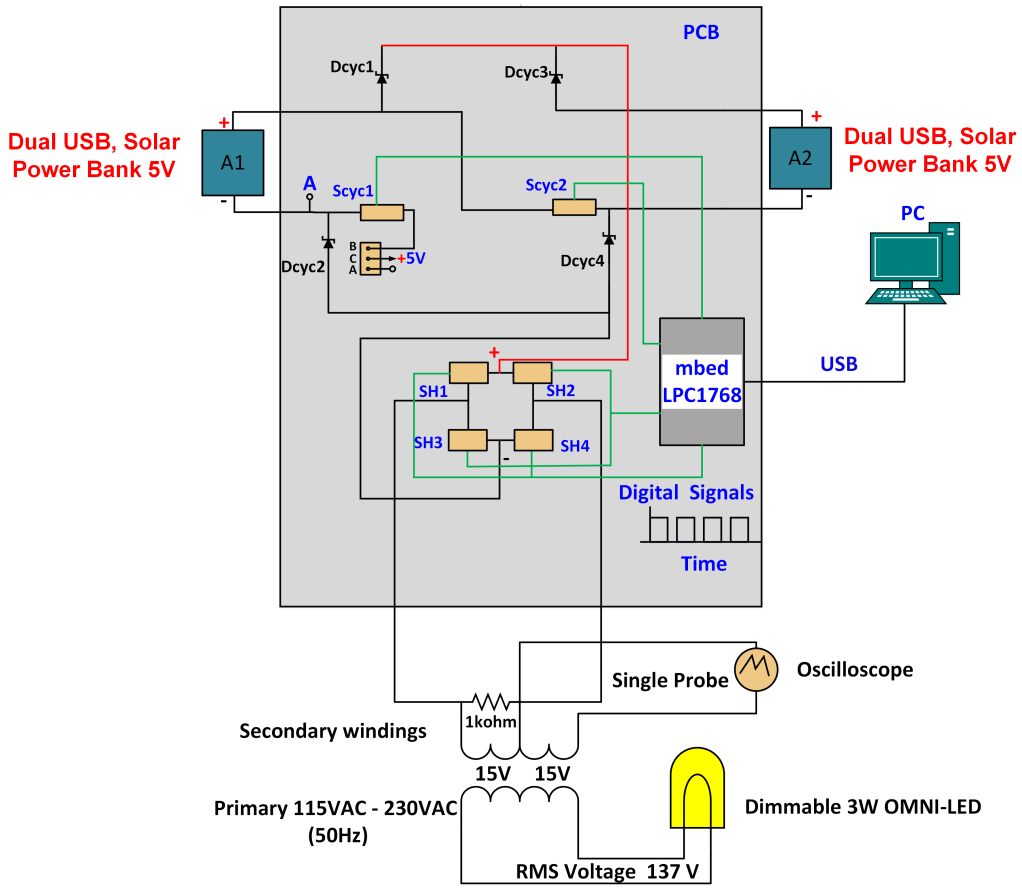

Figure 4.44: The revised setup of the 7-level cyclic selection inverter

The output waveform and its FFT spectrum are illustrated in Figure 4.45 and Figure 4.46 respectively.

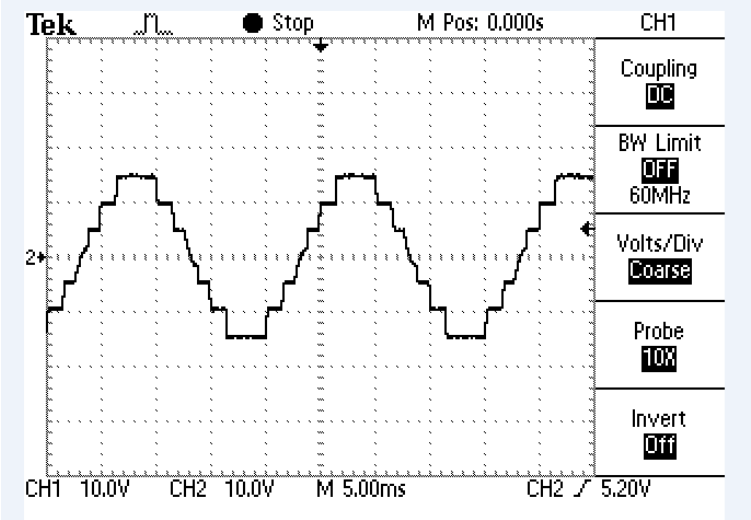

Figure 4.45: The AC staircase waveform output of the cyclic selection inverter (one scope probe) (Optimized timing steps)

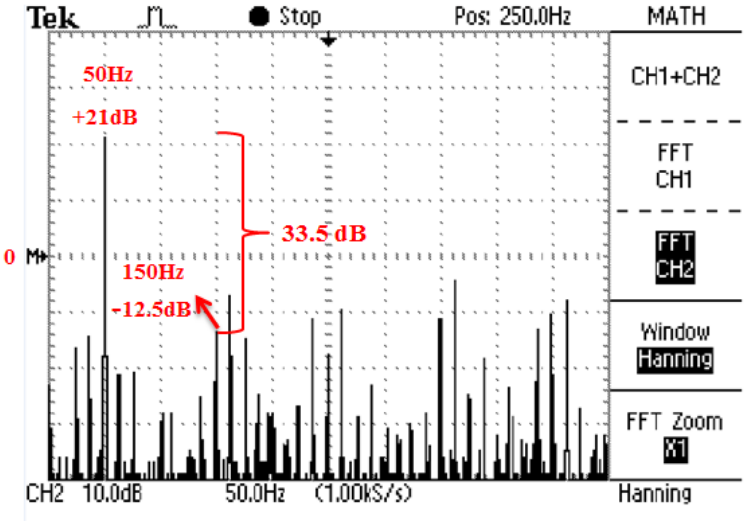

Figure 4.46: The fundamental and higher harmonics FFT spectrum of the cyclic selection inverter (Optimized timing steps)

The experimental seven-level cyclic inverter produced an excellent AC waveform with seven voltage levels and 27.18 V peak to peak voltage as shown in Figure 4.45. The FFT spectrum of the inverter shows that the difference between the fundamental

frequency (50 Hz) and the third harmonic (150 Hz) is 33.5 dB, revealing the expected harmonic reduction in the seven-level inverter due to the use of the timing steps optimization (Chapter 5). The total distortion of the output waveform (Figure 4.43) is calculated using equation 5.9. Thus, the THD is approximately 2.4% of the sine-wave power A^2.

In addition, the timing steps optimization method (Chapter 5) is compared to the equal timing steps method to highlight the reduction of the harmonic components. In this case, the time duration of each DC level of the cyclic selection output waveform in a quarter cycle (0 to 5 ms) is set to 1.25 ms as shown in Figure 4.47.

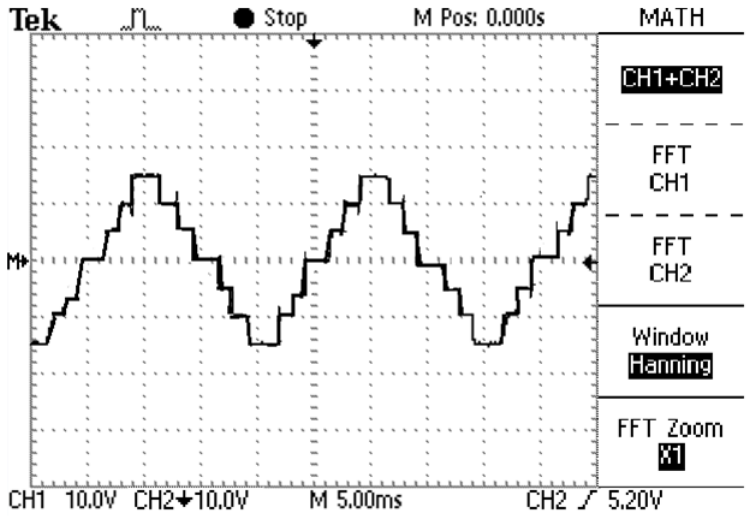

Figure 4.47: The AC staircase waveform output of the cyclic selection inverter (two scope probes in a differential mode) (equal timing steps)

The FFT spectrum and the output waveform of the the equal timing steps method are captured across 1 kΩ load of the cyclic selection inverter setup (Figure 4.44) by a single scope probe and displayed in Figure 4.49 and Figure 4.48 respectively.

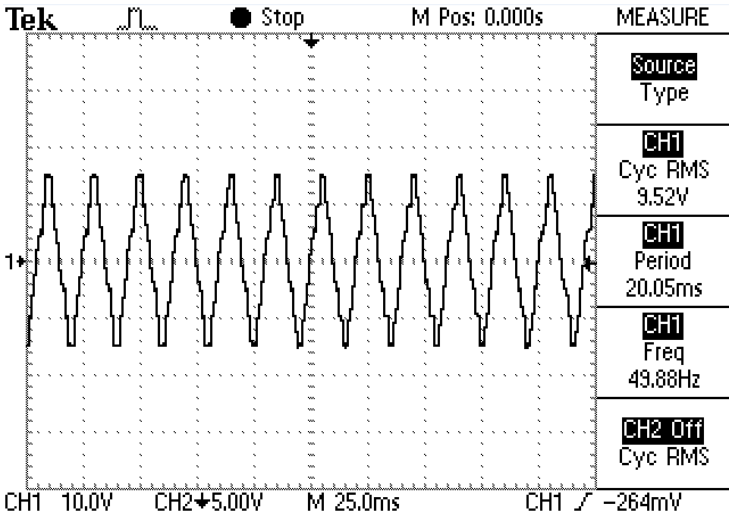

Figure 4.48: The AC staircase waveform output of the cyclic selection inverter (one scope probe) (equal timing steps)

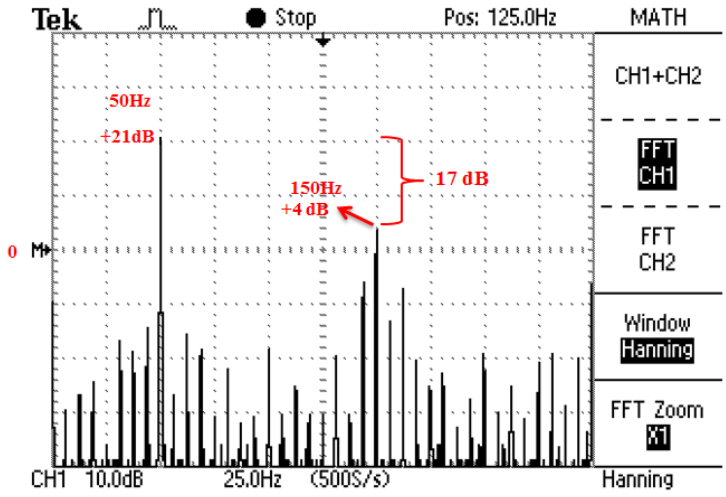

Figure 4.49: The fundamental and higher harmonics FFT spectrum of the cyclic selection inverter (equal timing steps method)

It can be concluded from Figure 4.46 and Figure 4.49 that the proposed optimization method (Chapter 5) has significantly minimized the harmonic components compared to the equal timing steps method. To highlight this, the third order component of the

proposed optimization method is approximately 2% of the fundamental component. However, the third harmonic component in the equal timing steps method is about 14.1% of the fundamental. The results show the excellent performance of the proposed optimization method.

4.7 Comparison of Golomb Inverter and Cyclic Selection Inverter

Table 4.14: The overall comparison of Golomb inverter and cyclic selection inverter

Golomb Inverter	Cyclic Selection Inverter
6 MOSFET Switches	7 MOSFET Switches
3 DC Sources	3 DC Sources
No Diodes	6 Diodes
No Capacitors (No Storage)	3 Batteries (Capacitors)
No Inductors	No Inductors
6 Levels without zero level	7 Levels including zero
Unevenly utilized DC sources	Evenly Utilized DC sources
Suitable for PV Application	Suitable for PV Application
Inverter-less	Inverter-less
Transformer-less	Transformer-less
Low Frequency Switching	Low Frequency Switching

Table 4.14 shows that the cyclic selection inverter outperforms the Golomb inverter by ensuring that the DC sources are evenly utilized. This is reached at the expense of higher circuit components compared to the Golomb inverter.

4.8 Conclusion

This chapter presented a DC-to-AC, seven-level, 50 Hz multilevel inverter for photovoltaic applications based on a cyclic selection algorithm. The number of levels of the output waveform of the proposed system here is not limited to seven; it can be adopted to a higher number of levels with an effective number of switching devices as already discussed in section 4.4.3. Although here all the discussions relates to low power applications, it can be applied to higher power applications like in grid-connected inverters.
The major advantage of the system here is that it gives a complete generation and storage and it has exactly the same performance as a PWM inverter.

The THD in the simulation results of the inverter differs from the experimental results. The difference can be accounted due to the Simulink limits in setting the required timing steps of the output voltage levels. It is not possible to model the timing steps of multilevel signals in the Simulink simulator. In the experimental results, the Mbed microcontroller is used to set the timing steps of each inverter to the required values.

The comparative study between the proposed inverters in this thesis shows that the cyclic inverter outperforms the Golomb inverter in terms of even source utilization.

CHAPTER 5

TIMING STEPS AND MPPT OPTIMIZATIONS

5.1 Introduction

In this chapter, a new mathematical method for determining the timing steps of the multilevel signals of known amplitude to minimize harmonic distortion is derived. This has the same performance as the well-known Fourier series method and require no carefully chosen starting point. The proposed method is based on a mean square error voltage regression theory which gives a real-time adaptive advantage. This

method can be used for an unlimited number of levels which is beyond the reach of computationally intensive Fourier methods.

It has been seen in Chapter 2 that conventional MPPT methods such as OP and hill climbing methods can fail under rapidly changing insolation levels. This is because of the fact that the actual power point is compared with one previous point only before a decision is made about the perturbation direction. Therefore, the operating point diverges from the MPP and will continue diverging under sudden change in the irradiance levels. To ensure that the MPP is successfully tracked even under sudden changes in atmospheric conditions, a novel direct control maximum power point optimizer using a forward-backward multiple step, load-side, current-mode sensing algorithm is proposed in this chapter. This technique maximizes the power into any given load using a current-mode, load-side controller under various insolation levels. This method uses a five-point comparison that compares the actual power point to two previous ones and two proceeding ones before a decision is made about the perturbation direction. The proposed method is based on load-side tracking technique unlike the conventional methods in which a PV side tracking is applied. The bueaty of load-side tracking which has the advantage of gu This method guarantees maximum power tracking under different weather conditions and operates at unity power factor on a self-synchronized basis.

5.2 Timing Steps Optimization

5.2.1 Optimization Aims and Previous Methods To Calculate Timing Steps

A critical step in designing multilevel inverters is the determination of the switching angles. The most common method is based on Fourier analysis and switching angle equation sets. These equations are developed to meet specific optimization aims. For instance, the minimization of the total harmonic distortion THD of the inverter output voltage or the elimination of lower order components of the load voltage [91]. These are generally non-linear transcendental equations which require iterative methods such as Newton-Raphson with multiple variables, a method based on theory of symmetric polynomials and resultants, and methods based on genetic algorithms to solve them [91], [92]. In [93], Fourier approximation of a five-level multilevel inverter was demonstrated to determine the switching instants with minimum distortion. This suggests the use of equal steps level and then the optimization of the values of the switching angles for minimum distortion or entirely eliminating the third order harmonic at an expense of slightly higher THD [93]. One of the dominated drawbacks of the Fourier series method is that the optimization starting point is required to be carefully chosen. This method suffers also from the imperfections near the discontinuity of overshooting and undershooting the function value which is known-mathematically as the Gibbs phenomenon. The effect of the Gibbs phenomenon in a Fourier approximated signal is shown by illustrating an example of the 1000^{th} partial Fourier sum of the pulse function as in Figure 5.1 and Figure 5.2.

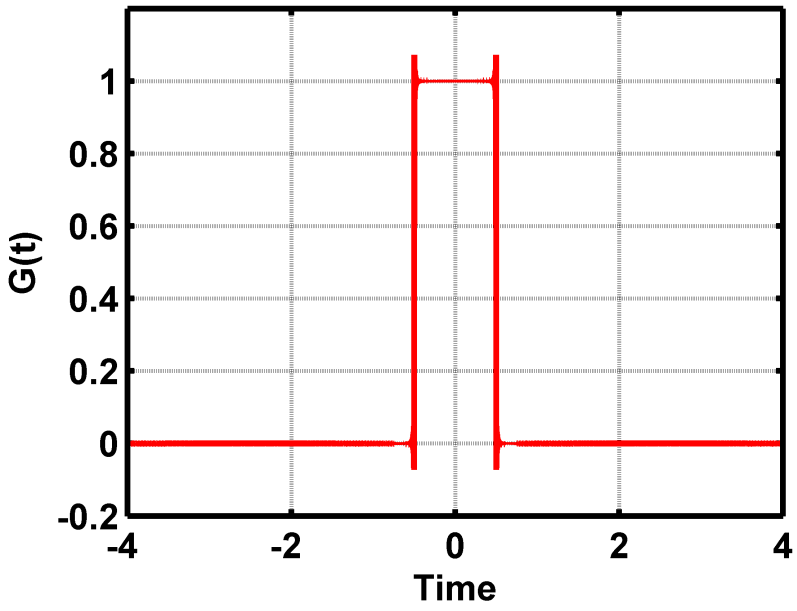

Figure 5.1: 1000^{th} partial Fourier sum of the pulse function

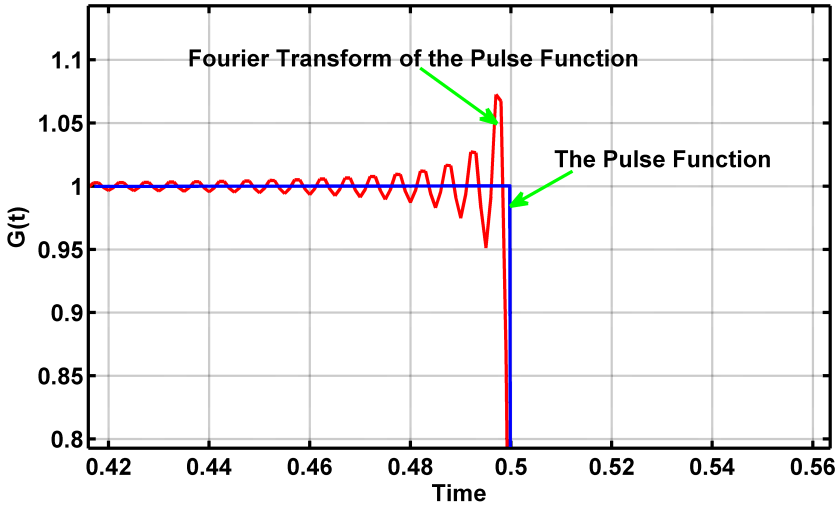

Figure 5.2: The Gibbs phenomenon in the pulse function

It is very obvious from Figure 5.2 that the fundamental amplitude of the partial sums overshoots and undershoots the amplitude of the pulse function. As more and more

terms of partial sums are added, away from the discontinuity, the approximation begins to resemble the pulse function. This is however very time consuming and it can only be obtained by means of an offline operation. Clearly, calculations based on Fourier and equations sets methods are computationally intensive and therefore they cannot be implemented in real-time. Few attempts have been made to implement real-time algorithms by a microprocessor to determine switching angles. A simple algorithm was proposed in [92] to obtain the switching angle in real-time for step modulation. It makes use of the voltage second areas of the divided reference voltage according to the output levels of the inverter. The method overcomes the computationally intensive of Fourier and equation sets methods, but it calculates a number of trigonometric functions which can be done in real-time [91]. However, this method cannot guarantee minimizing THD or eliminating lower order components. The calculations based on this method are obtained through an online operation [91].

In this section, a completely new mathematical method for determining the switching angles and the timing steps of the multilevel inverter with known-amplitude so as to minimize harmonic distortion is described. In fact, there are various optimization aims for different applications, which are either 1) eliminating the lower order odd harmonic components in the load voltage, such as the third, fifth, seventh etc., or 2) minimising total harmonic distortion THD. The latter is widely preferred in photovoltaic applications [91].

The proposed method here has three unique characteristics. First, the voltage THD is proven mathematically to be minimum and thus additionally minimizes each harmonic component. Second, it gives the same performance as the well-known Fourier

series method but requires no carefully chosen optimization starting point. Lastly, this method is real-time adaptive and can be used for an unlimited number of levels which is beyond the reach of computationally intensive Fourier methods.

5.2.2 A Theoretical, Mathematical and Mean Square - Error Voltage - Based Approach

The proposed timing steps method here is based on a mean square-error voltage regression theory that minimizes THD in the stepping waveform signal. This approach finds the global best point unlike the well-known Fourier series method which requires carefully chosen optimization starting point. This method obtains the switching angles and timing steps of the multilevel signal of known-amplitude by finding the mean-square error voltage MSEV for the segmented waveform from sine-wave $A\sin(\theta)$ in the range 0 to $\frac{\pi}{2}$. The mean-square error voltage measures the average of the squares of the errors which is the difference between the estimator (sine-wave) and estimated voltage (multilevel steps). This method can be applied in two different scenarios as:

1. Variable Time and Amplitude

2. Amplitude dependent on Time

A multilevel approximation to half-period of a sine-wave $A\sin(\theta)$ (where: $0 \leq \theta \leq \pi$) is shown schematically in Figure 5.3. Only three levels are shown for analysis purposes with no loss of generality.

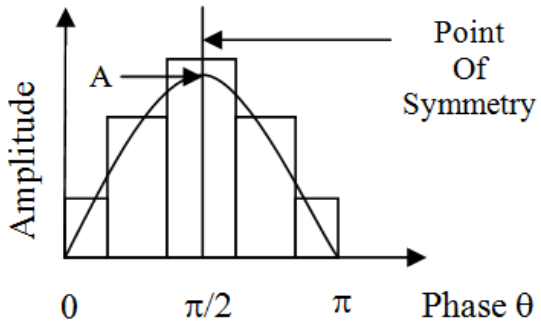

Figure 5.3: Segmented sine-wave showing axis of symmetry

Figure 5.3 can be redrawn as in Figure 5.4 showing just the first $\pi/2$ segment as the $\pi/2$ to π segment is a mirror image and the π to 2π region is a simple inversion.

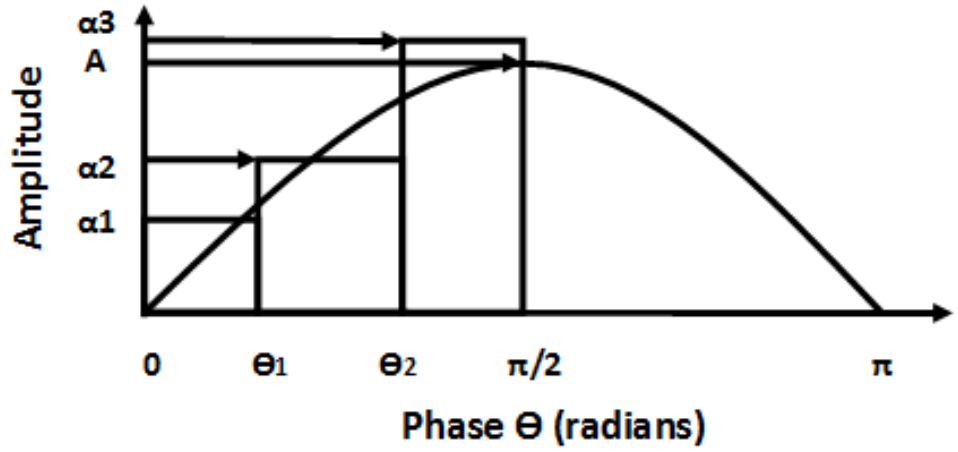

Figure 5.4: Zero to $\pi/2$ sine-wave segment

It can be seen in the simplified case of Figure 5.4, that there is a choice of three amplitudes (including zero) and two phase markers: α_1, α_2, α_3, and θ_1, θ_2 respectively. Next, the mean-square error voltage (MSEV) D(α_1, α_2, α_3,θ_1, θ_2,A) for the segmented waveform from the sine-wave in the range 0 to $\frac{\pi}{2}$ is determined as in equation (5.1).

A is the required sine-wave amplitude.

$$D(\alpha_1, \alpha_2, \alpha_3, \theta_1, \theta_2, A) = \frac{\pi}{2}[\int_0^{\theta_1} (A\sin(\theta) - \alpha_1)^2 d\theta + \int_{\theta_1}^{\theta_2} (A\sin(\theta) - \alpha_2)^2 d\theta + \int_{\theta_2}^{\frac{\pi}{2}} (A\sin(\theta) - \alpha_3)^2 d\theta] \tag{5.1}$$

It is possible now to minimize equation (5.1) with respect to any of the five free parameters for the required sine-wave amplitude A (chosen for minimum distortion). In other words, one can find θ_1 and θ_2 given α_1, α_2, α_3 or vice-versa. After some manipulation using symbolic algebra software, the simple results in equations (5.2)-(5.6) below were obtained.

$$\sin(\theta_1) = (\frac{\alpha_1 + \alpha_2}{2A}) \tag{5.2}$$

$$\sin(\theta_2) = (\frac{\alpha_2 + \alpha_3}{2A}) \tag{5.3}$$

$$\alpha_1 = A(\frac{1 - cos(\theta_1)}{\theta_1}) \tag{5.4}$$

$$\alpha_2 = A(\frac{\cos(\theta_1) - cos(\theta_2)}{\theta_2 - \theta_1}) \tag{5.5}$$

$$\alpha_3 = A(\frac{cos(\theta_2)}{\frac{\pi}{2} - \theta_2}) \tag{5.6}$$

A straightforward generalization is possible as in equation (5.7) and equation (5.8)

$$\theta_n = \sin^{-1}(\frac{\alpha_n + \alpha_{n+1}}{2A}) \tag{5.7}$$

$$\alpha_n = A(\frac{\cos(\theta_n) - cos(\theta_{n+1})}{\theta_{n+1} - \theta_n}) \tag{5.8}$$

where $(\alpha_n + \alpha_{n+1})$ is the average value. The MSEV can then be written in closed form as in equation (5.9)

$$MSEV = \frac{\pi}{4}(A^2 + 2\alpha_N^2) - \sum_{n=1}^{N}[2A(\alpha_n - \alpha_{n-1})\cos(\theta_{n-1}) + \theta_{n-1}(\alpha_n^2 - \alpha_{n-1}^2)] \quad (5.9)$$

where N is the total number of steps in a quarter period (0 to $\frac{\pi}{2}$). A is the best maximum available amplitude.

To obtain a numerical result, it is assumed that: α_1, α_2, and α_3 are 100, 200, and 300 volts, respectively and that $A = 325$ volts (i.e., a standard 230 VAC waveform). Using equation (5.7) and equation (5.8), produces $\theta_1 = 0.479$ rad and $\theta_2 = 0.877$ rad. The total distortion from equation (5.9) is just 1.8% of the sine - wave power. It may be noted that this value is very similar to that of uniform amplitude and time quantization. The advantage of this new method being that amplitude and time steps can be chosen in real - time to suit the user's voltage and time constraints. From the characteristics of the quantization distortion as a function of a signal level, the signal to noise ratio SNR is given by SNR quantization equation in (5.10).

$$SNR = (6.02n_{bit} + 1.76)dB \quad (5.10)$$

where n_{bit} is the number of bits of the quantizer.

It can also be stated that the MSEV reduces as N^2 as illustrated in Table 5.1. Table 5.1 shows an example of 1, 2, 3, 4, and 5 number of steps in a quarter cycle analysis to illustrate the total distortion TD in percentage % of the chosen sine - wave amplitude of 125 V, 225 V, 325 V, 425 V, 525 V respectively.

Table 5.1: The total distortion (%) and MSEV at different N levels

N	A	α_1	α_2	α_3	α_4	α_5	MSEV	TD (%) of the sine - wave power A^2
1	125	100	-	-	-	-	2979.8	19
2	225	100	200	-	-	-	2159.8	4.2
3	325	100	200	300	-	-	1859.7	1.8
4	425	100	200	300	400	-	1708.8	0.94
5	525	100	200	300	400	500	1615.6	0.58

It can be deduced from the Table 5.1 that the total distortion when N = 1 is approximately 19% while it is only 0.947% and 0.58% at N = 4 and N = 5 respectively. In fact, the quarter cycle angle is fixed at $\frac{\pi}{2}$ in one level waveform (square-wave) and thus no angular optimization is applied. Figure 5.5 shows the relationship of the distortion TD to the number of steps in quarter cycle N. The total distortion in fact decays in a negative exponential manner as N increases as shown in Figure 5.5.

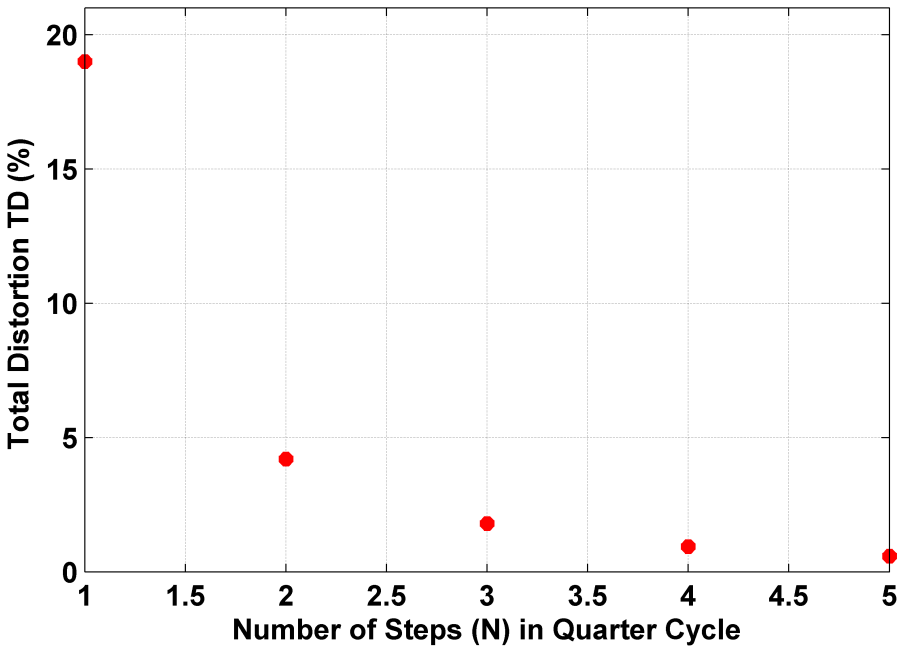

Figure 5.5: The relationship between TD and N at various A amplitudes

It is clear from Figure 5.5 that TD at N = 5 is over 30 times lower than that at N = 1. Comparing the distortion represented by equation (5.9) and equation (5.10), it may be seen in Table 5.2 that equation (5.9) gives a similar results with good accuracy to equation (5.10). It is worth noting that SNR improves by 6.02 dB per bit.

Table 5.2: Comparisons of SNR and TD of MSEV in (%) at various N levels

N	A	α_1	α_2	α_3	α_4	α_5	SNR %	TD %
1	125	100	-	-	-	-	16.6	19
2	225	100	200	-	-	-	4.1	4.2
3	325	100	200	300	-	-	1.8	1.8
4	425	100	200	300	400	-	1	0.94
5	525	100	200	300	400	500	0.66	0.58

Applying the theoretical MSEV approach proposed here to the modified square-wave signal of 1 V amplitude as depicted in Figure 5.6.

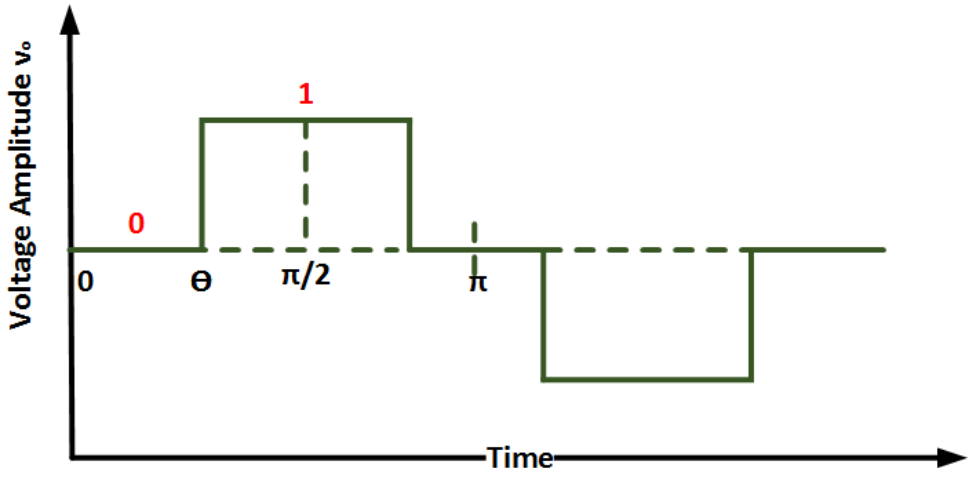

Figure 5.6: A modified square-wave signal

θ in Figure 5.6 can be determined from equation (5.7) with A=1 as follows:

$$\theta = \sin^{-1}(\frac{0+1}{2}) = 30^{\circ} \tag{5.11}$$

The quasi square-wave shown in Figure 5.6 has both half-wave and quarter-wave symmetries, the integration of the Fourier analysis is only required over one quarter period from 0 to $\frac{\pi}{2}$. This means only sine terms and odd components (n= 1,3,5,...,) are required as in equation (5.12):

$$\begin{aligned} b_n &= \frac{4}{\pi}[\int_0^{\alpha} v_o sin(n\omega t)d(\omega t) + \int_{\alpha}^{\frac{\pi}{2}} v_o sin(n\omega t)d(\omega t)] \\ &= \frac{4}{n\pi}\left[-cos(n\omega t)\right]_{\alpha}^{\frac{\pi}{2}} \\ &= \frac{4}{n\pi}cos(n\alpha) \end{aligned} \tag{5.12}$$

Substituting the value of (θ) given in equation (5.11) into equation (5.12), results in $b_n = 0$ for $n = 3$.

The Fourier coefficients b_n at odd frequencies and a_n at even frequencies against frequency for the modified square-wave are displayed in Figure 5.7. The spectrum analysis $|c_n|$ of the modified square-wave is shown in Figure 5.8.

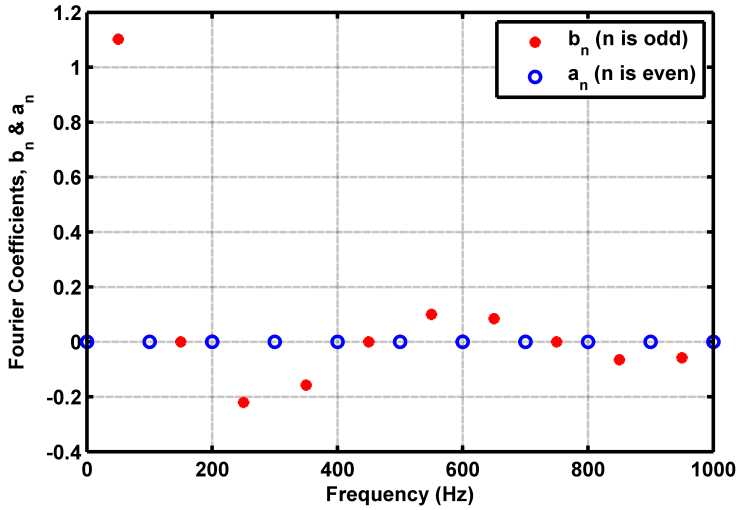

Figure 5.7: Fourier coefficients of the modified square-wave signal

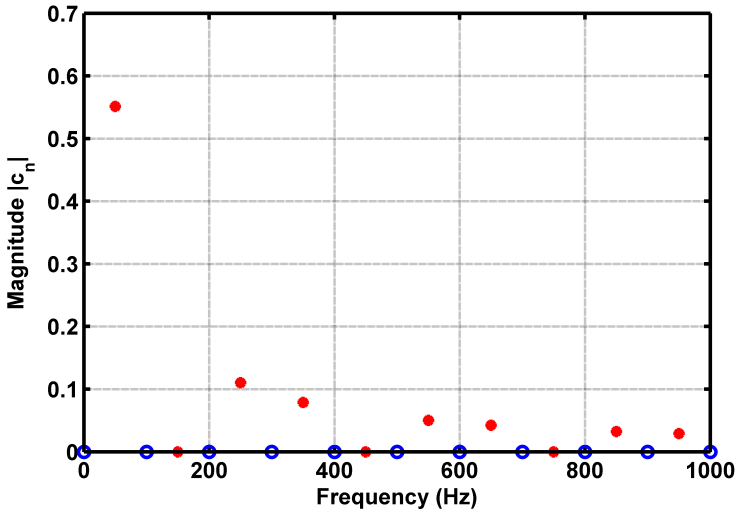

Figure 5.8: Magnitude spectrum $|c_n|$ of the modified square-wave

It can be concluded from the harmonic analysis that the third harmonic b_3 is entirely eliminated from the modified square-wave signal by using the proposed method as it is the hardest to filter out. The proposed method requires no carefully chosen optimization starting point. The total harmonic distortion of an odd symmetry waveform is defined by equation (5.13) [93].

$$THD = \frac{[\sum_{n=3}^{n=\infty}(b_n)^2]^{\frac{1}{2}}}{b_1} \tag{5.13}$$

Numerical evaluation of the coefficients for the modified square-wave indicates that if the modified square-wave is to be considered as a sine-wave with distortion, the THD of the modified square-wave is in the range of 28% (-11 dB). The third harmonic of the modified square-wave is 0% of the fundamental.

The optimization method of determining the switching angles and timing steps here can be obtained in real-time with less computational complexity and used for an

unlimited number of levels which is beyond the computationally intensive Fourier methods. It has been proven in this section that the voltage THD is minimized by the proposed mathematical approach.

5.3 Load - Side, MPPT Optimizer

5.3.1 Principle of Operation

Most recent applications of MPPT are based on the PV side using power converters with no attention to load protection as shown in Figure 5.9. A lossy power converter stage between the supply side and load side causes a failure in delivering the maximum power to the load. In fact, the load must be chosen correctly to absorb all the delivered power from the PV source. However, the characteristics of a load in some applications are continuously varying. This necessitates applying the MPPT at the load side to overcome all the significant issues of over current or over voltage at any given load as shown in Figure 5.10.

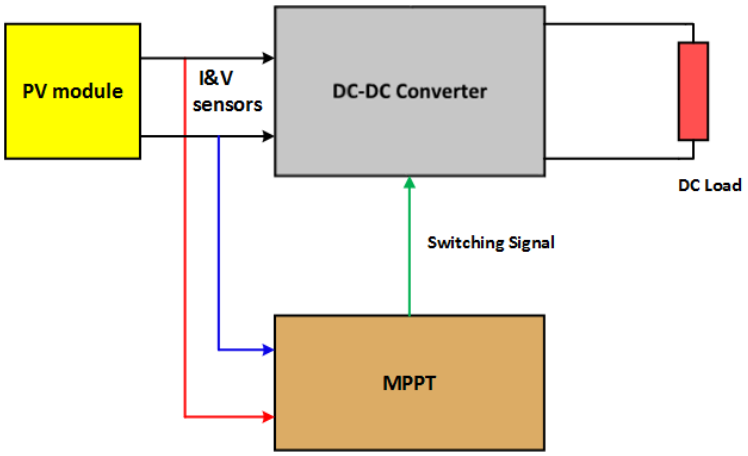

Figure 5.9: Block Diagram of conventional MPPT

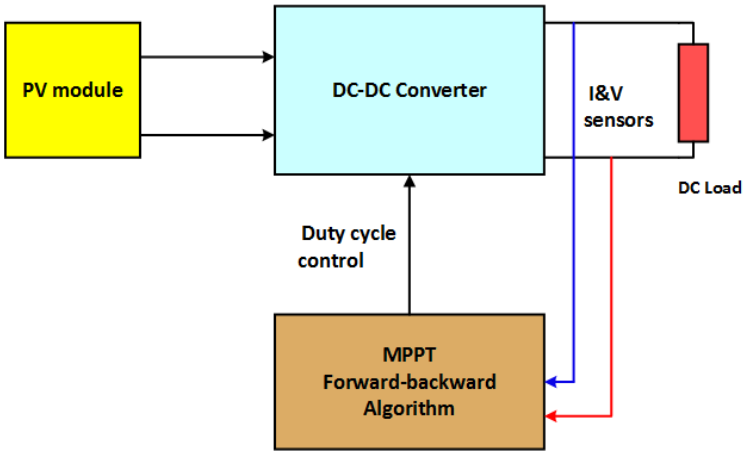

Figure 5.10: Block Diagram of proposed MPPT

Unlike conventional MPPT methods based on PV side sensing (PV voltage or current) as illustrated in Figure 5.9, the proposed MPPT method is based on load side power maximization. This means that the power of the intermediate stage (DC to DC converter) is maximized into any given load. This technique enhances the tracking procedure because the optimum power delivered from the PV source through the power converter the intermediate stage to the load is guaranteed. The control

approach adopted here senses a single load parameter (current) which leads to a reduction in the required sensors and further simplifies the control algorithm. An attempt at a load side optimization has been described using a conventional PO algorithm, which was compromised by varying solar irradiation levels [94]. One of the basic problems with a conventional PO algorithm is that this will fail to track the MPP under sudden drop in irradiance level as it checks either one point forward or one point backward. The algorithm will reduce the voltage in the wrong direction that leads to more power dissipation and losses as discussed in details in Chapter 2. In the present context, a multiple step, forward-backward algorithm based on first derivative central difference theory is applied to solve the problems of the conventional MPPT algorithms and guarantees the maximum power under rapidly changing atmospheric conditions.

Figure 5.10 shows that the PV module is connected to a DC to DC converter to match the PV module internal impedance to any given load and adjust the operating condition to reach the maximum power point. It is worth noting that the PV module cannot transfer maximum power to the load itself due to an impedance mismatch. The converter is used in current mode by altering the duty cycle to maximize the current into any given load. The algorithm stopped tracking when maximum current and hence power, is reached.

5.3.2 Multiple Step, Forward - Backward Algorithm

As mentioned in Chapter 2, the conventional direct MPPT control methods can fail and track in wrong direction under rapidly changing weather conditions. Here, a mul-

tiple step central difference MPPT algorithm which successfully tracks the position of the MPP at various irradiance conditions and maximizes the power into any given load is proposed.

An attempt has been made to apply the central differentiation algorithm using a single step scheme to improve the performance of MPPT by Xiao et al [95]. However, this follows the conventional PV side control methods where the output voltage of the PV side is maximized. In this work, however, a multiple step forward - backward difference scheme is used to accurately approximate the numeral derivative of a function at any point. In fact, the truncated error of Taylor series in the multiple step scheme decreased by half compared to the single step analysis.

Multiple step central difference algorithm (multiple step forward - backward) is symmetric and requires five point measurements: (R_{i-2}, P_{i-2}),(R_{i-1}, P_{i-1}), (R_i, P_i), (R_{i+1}, P_{i+1}) and (R_{i+2}, P_{i+2}) to estimate the derivative value at the centre point (R_i, P_i) and find the MPP unlike the single step algorithm where only three point measurements are required. P_i , P_{i-1}, and P_{i+1}, P_{i-2} and P_{i+2} symbolize the sequence of DC to DC converter output power, and R_i , R_{i-1} , R_{i+1}, R_{i-2} and R_{i+2} represent the equivalent impedances seen by the PV panel. This technique is capable to direct any point on the P - R curve as shown in Figure 5.11 towards the MPP by checking two points in both directions (forward - backward) of any particular point in order to make the right decision under various weather conditions. For instance, the power at point (A) is checked against two, one - sided backward points and one - sided, two forward points to make the right decision at any insolation level. This method guarantees tracking under all the possible scenarios: the point is up the hill, the MPP,

down the hill with increasing or decreasing insolation levels.

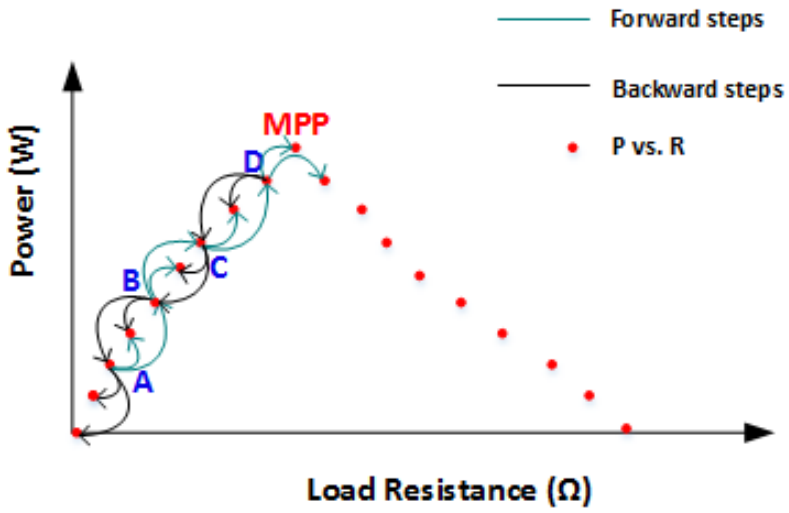

Figure 5.11: The operation principle of the multiple-step, forward-backward MPPT algorithm

The numerical derivative of the function of the P - R curve at any point on its graph can be approximated by neighbourhood points using either forward, backward or central finite difference methods. In a single step scheme, the first - order, one - sided backward, one - sided forward and two - sided central - differentiation mathematical formulas using two - points that are evenly spaced at $(\triangle R)$ are given by equations (5.14), (5.15) and (5.16) respectively.

$$\text{Backward Method} \rightarrow f'(R_i, P_i) = \frac{P_i - P_{i-1}}{\triangle R} \tag{5.14}$$

$$\text{Forward Method} \rightarrow f'(R_i, P_i) = \frac{P_{i+1} - P_i}{\triangle R} \tag{5.15}$$

$$\text{Central Method} \rightarrow f'(R_i, P_i) = \frac{P_{i+1} - P_{i-1}}{2 \triangle R} \tag{5.16}$$

where, (R_i, P_i) is the point of interest. (R_{i-1}, P_{i-1}) is the point of the interest minus

step size (backward point); (R_{i+1}, P_{i+1}) is the point of the interest plus step size (forward point); $2 \triangle R$ is the distance between the forward and backward points; $\triangle R$ is the incremental step of the equivalent impedance seen by the PV (adjusted by duty cycle of the converter (D)).

The first order formulas using the single step scheme are only using two points and are not as accurate as they can be if all three data points are used. The truncated errors in equations (5.14) and (5.15) is $O(\triangle R)$ while it is $O(\triangle R)^2$ in equation (5.16). Likewise, the first - order one - sided backward (three points), one - sided forward (three - points) and two - sided central - differentiation (four - points) mathematical formulas using multiple step scheme are given by equations (5.17), (5.18) and (5.19) respectively. (It is worth noting that the points are evenly spaced at $\triangle R$).

$$\text{Backward Method} \rightarrow f'(R_i, P_i) = \frac{3P_i - 4P_{i-1} + P_{i-2}}{2 \triangle R} \tag{5.17}$$

$$\text{Forward Method} \rightarrow f'(R_i, P_i) = \frac{-3P_i + 4P_{i+1} - P_{i+2}}{2 \triangle R} \tag{5.18}$$

$$\text{Central Method} \rightarrow f'(R_i, P_i) = \frac{P_{i-2} - 8P_{i-1} + 8P_{i+1} - P_{i+2}}{12 \triangle R} \tag{5.19}$$

A function $f(R, P)$ can change from increasing to decreasing at which the tangent line is parallel to the x-axis, and therefore the derivative at this point is zero, is called the maximum point. The truncated errors in equations (5.17) and (5.18) is $O(\triangle R)^3$ while it is $O(\triangle R)^4$ in equations (5.19). The latter gives a high resolution and reasonable accuracy on finding the MPP point.

For the multiple step scheme, it is required to find the point where $f'(R, P) = 0$:

$$\frac{dP}{dR} = 0 \tag{5.20}$$

When the calculations in the multiple step scheme show that, the differentiation approximation of $f(R_i, P_i)$ for the multiple step case is very close to zero and the MPP is located at the centre point instead of (P_{i+1}, R_{i+1}), (P_{i-1}, R_{i-1}) ,(P_{i+2}, R_{i+2}) or (P_{i-2}, R_{i-2}).

Recall that (R_i,P_i) is the point of interest on the P-R curve; and this acts as a critical point when the slope of a function is zero at that point. Suppose that (R, P) is a point on the P-R curve and the first derivative at this point $f'(R, P)$ is negative which means that the function $f(R, P)$ is decreasing at that point. Positive slope indicates that the function $f(R, P)$ increases at the (R, P). Zero slope at $P_{i-2} - 8P_{i-1} + 8P_{i+1} - P_{i+2} = 0$ indicates that the function is at the MPP. In fact, the maximum power point is located at the centre point (R_i, P_i) instead of either (R_{i-2}, P_{i-2}),(R_{i-1}, P_{i-1}), (R_{i+1}, P_{i+1}) or (R_{i+2}, P_{i+2}). The controller stops tracking once the MPP is located and thus reduces the ripples in the output power compared to continuous PO tracking. The truncated error of one-sided three point backward, forward methods is $O(\triangle R)^2$ while it is $O(\triangle R)^4$ in the two-sided central four-points. The latter means that the error is only $\frac{1}{8}$ compared to $\frac{1}{4}$ error in the central method using the single step scheme.

The flowchart in Figure 5.12 demonstrates an implementation of the proposed multiple step, forward-backward algorithm. The main difference between the proposed control system and the existing one is that, instead of sensing the current and the voltage output of the PV panel, the output current of an intermediate stage (DC to DC converter) is maximized at any given load under various irradiance levels. Thus maximum output current implies maximum power for all load types except current source where power may be maximized by maximizing the output voltage.

The numerical differentiation is based on multiple points centred difference according to the analysis mentioned above.

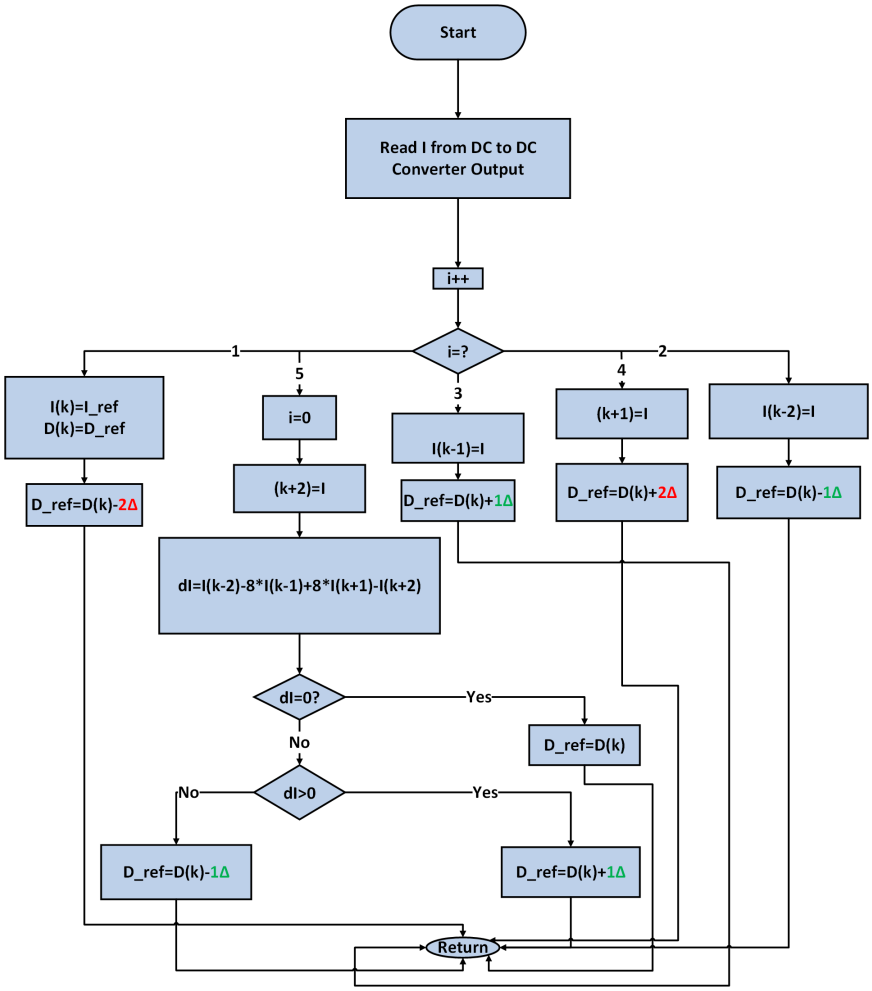

Figure 5.12: Flowchart of the multiple step, forward-backward Algorithm

dI in Figure 5.12 is the derivative of the converter output current. $I(i)$ and $D(i)$ are the DC to DC converter output current and duty cycle at instant (i). $\triangle$ is the step size which is manually adjusted to read $I(i)$, $I(i-2)$, $I(i-1)$, $I(i+1)$ and $I(i+2)$. The variable (k) is used for scheduling the computation load of MPPT.

$I(i)$, $I(i-2)$, $I(i-1)$, $I(i+1)$, and $I(i+2)$ are the output current of DC-to-DC

converter at instant (i), at two previous instants $(i-2)$ & $(i-1)$, and two forward instants $(i+2)$ & $(i+1)$, respectively.

It is clearly shown in the flowchart that the proposed algorithm requires five - point measurements and the central differentiation function is evaluated in each cycle according to the criteria. This algorithm shows that if the output current of DC to DC converter at $I(i+2)$ and $I(i+1)$ are greater than $I(i-2)$ and $I(i-1)$, then the direction is maintained, otherwise it is reversed. Thus the current is increased through $D_{ref} = D(i) + 1\triangle$ while it is decreased through $D_{ref} = D(i) - 1\triangle$.

5.3.3 MPPT Converter Choice

The PV module cannot transfer maximum power to the load itself due to an impedance mismatch. A DC to DC converter is utilized to match the PV module internal impedance to any given load and adjust the operating condition to reach the maximum power point. To maximize the power into any given load above or below the supply source, a buck-boost converter is consequently selected.

At a steady state and assuming the converter is operating in continuous mode, the relationship of the current and voltage at the load terminals with those at the PV system are displayed in equation (5.21) and equation (5.22).

$$V_o = \frac{D}{1-D} V_i \tag{5.21}$$

$$I_o = \frac{D}{1-D} I_i \tag{5.22}$$

where, D is the converter duty cycle, I_i is the PV current, I_o is the load current, V_o is the load voltage, and V_i is the PV voltage.

Thus, the load resistance can be written as (5.23) while the equivalent resistance seen by the PV system displayed in equation (5.24).

$$R_L = \frac{D^2}{(1-D)^2} R_i \tag{5.23}$$

$$R_i = \frac{(1-D)^2}{D^2} R_L \tag{5.24}$$

where, R_i the equivalent impedance seen by the PV system, and R_L is the load impedance.

It is clear from equation (5.24) that for a certain load resistance the equivalent resistance depends only on the duty cycle of the buck boost converter. Thus, to maximize the power into a load the duty cycle is adjusted.

5.3.4 Experimental Implementation of MPPT

5.3.4.1 Overall Layout

The laboratory implementation layout for the maximum power point optimizer is shown in Figure 5.13. The major components of the setup are an off-the-shelf 4 - 32V to 0.8 - 32V four-switch, DC-to-DC buck boost non-inverting converter along with a controllable, indoor, built-in-house, solar simulator system. The converter matches the PV module internal impedance to any given load. A buck-boost converter could transfer energy to load above and below the supplied source voltage. This converter

controls current as well as voltage using a built-in potentiometers.

Here, the converter is connected to a resistive load of 1Ω, and the load voltage is controlled by adjusting the duty cycle of the power converter using the voltage potentiometer and setting the current at maximum using the current potentiometer to ensure that the converter is operating in current mode. The load current is observed using a USB digital multimeter and MATLAB provides data processing (MATLAB code is included on a CD). The LED floodlight source of the solar simulator is controlled by LPC1768 Mbed microcontroller to set the intensity of the light to any given value within the LED floodlight capabilities ($78 W m^{-2}$ maximum, $\sim$ 0.08 of 1 sun).

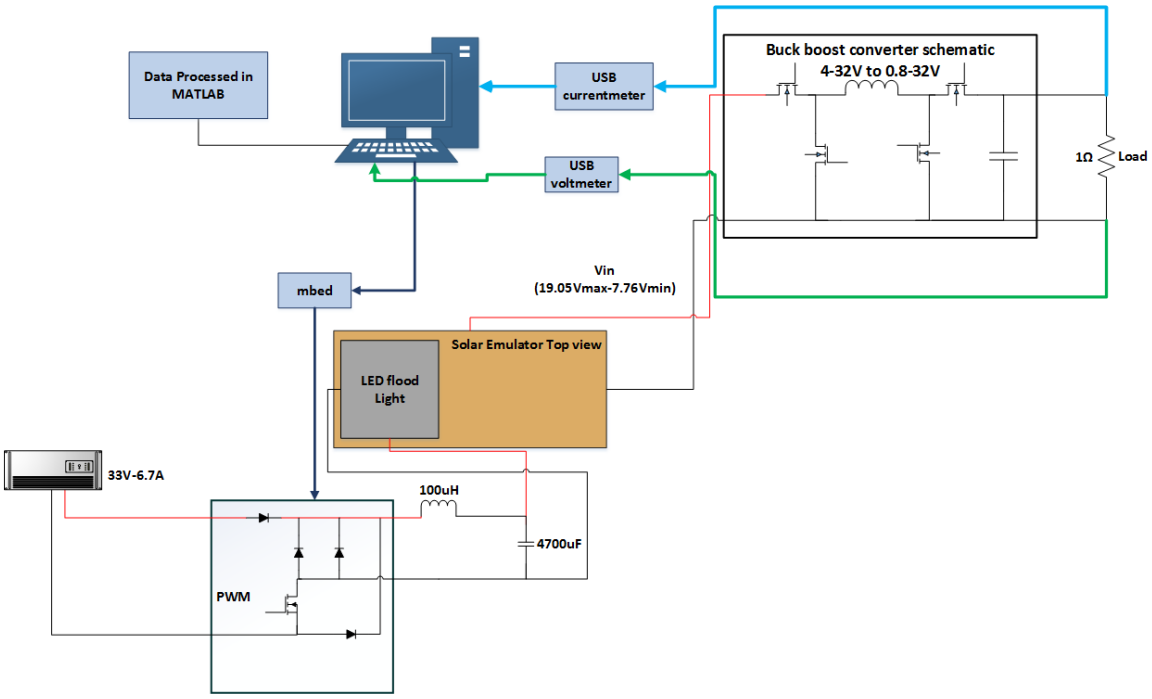

Figure 5.13: The implementation layout of the proposed MPPT optimizer

5.3.4.2 Main Component Selection and System Design

5.3.4.2.1 PV Module and Light - Source Selection

A low-cost indoor solar simulator is designed and constructed in this project to offer a laboratory test and control facility to Multicrystal Photovoltaic (KD70SX-1P) module. KD70SX-1P module is the core of the solar simulator which has high performance integrated solar cells with over 16% efficiency and contains 36 polycrystalline solar cells. Various light sources have been used in the history of solar simulators such as: carbon arc lamp, metal halide arc lamp, quartz tungsten halogen lamp, xenon arc lamp, mercury xenon lamp, argon arc lamp and light emitting diode (LED) [96]. An LED is a semiconductor light source which emits a narrow-spectrum of light when biased in the forward direction of the p-n junction electrically. The emission mechanism of the LEDs are not the same as an arc lamp or a filament lamp.

LEDs were mainly used as indicators and signs with a low intensity in the early days. The market for the high power LED solutions started in the early 2000s, LEDs were utilized as a illumination source for solar simulators [96]. LEDs have more advantages compared to the conventional light sources. LEDs can be operated at one light output intensity and controlled very fast, these are also available with a variety of colours and wavelengths, and are more compact and energy saving. LED can offer high intensity reaches ($1000 W/m^2$) and more. They also have in general very long lifespan up to 50,000 and 100,000 hours which could reduce the maintenance cost to a minimum. LEDs solar simulators can be designed with small size concentrator with a low cost unlike the conventional light sources [96]. Having said that, however, the light output energy efficiency and lifetime of LEDs are affected by temperature and thus the heat

transfer devices are required. Another drawback point is that the light intensity of the LEDs is still low for a concentrating solar simulator [96].

The advantageous of LEDs greatly outweigh the disadvantages and in order to reap these benefits, an off-the-shelf, high power (200 W) LED floodlight with luminous flux of 17800 lumen and 4 COB LEDs (Chips on Board) with a built-in aluminium heat sink and DC power supply is selected here as an illumination source of the solar simulator.

5.3.4.2.2 Solar Simulator Construction and Design

Mechanically, the complete design of solar simulator consists of a lightweight wooden enclosure which has a trapezoid cross sectional area. The enclosure constructed of two main parts. The first part is the main body of the enclosure which has a truncated pyramid shape to concentrate the light rays. The LED floodlight with its built-in aluminium heat-sink is mounted at the top of the truncated body. The second part of the enclosure is a frame type of base with four caster wheels to hold one PV module that is supported by a small side rail cleats. The two parts are joined using metal hooks. The internal surrounding of the enclosure is covered by a thermal insulation layer. This surrounding offers a layer of insulation air bubbles with a thermally reflection aluminium surface on the front face which reduces the intensity losses. The LED floodlight position was adjusted in order to achieve the optimum PV current output with the maximum LED intensity. The distance between the PV module and the light source is optimized along with the position to obtain the optimal PV output with the maximum available light intensity. Figure 5.14 gives an overview of the complete design of the solar simulator. Figure 5.15 shows the complete hardware

design.

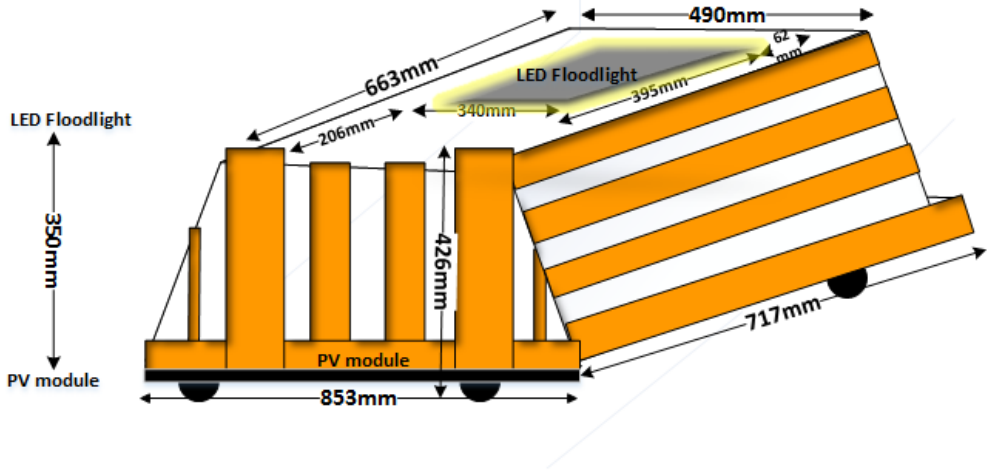

Figure 5.14: Schematic of the designed solar simulator

Figure 5.15: The top view of the solar simulator hardware

Figure 5.14 shows that the optimum height between the light source and the PV module is 350 mm at which the PV module output current is optimized. The hight

between the light source and the PV module is optimized to increase the efficiency of the solar simulator. The overall maximum light intensity of the source within the enclosure that is absorbed by the PV module is approximately 1/10 of the sun. This is about 78.4 W/m^2 according to the I-V curve of the selected PV module [97].

The specification given by [98] showed that the LED floodlight has a mean of 6000 K correlated colour temperature. The peak wavelength of this LED floodlight can be extracted from Wien's displacement law as in below:

$$\lambda = \frac{2.898 \times 10^{-3}(m.K)}{T(K)} \tag{5.25}$$

where, T is LED correlated colour temperature in Kelvin (T= 6000 K in this case), λ is peak wavelength of the LED (483 nm). This is with good agreement with the cool white spectrum at which more blue light issued at a wavelength approximately 483 nm. Further, the luminous efficacy of the eye response as a function of frequency is approximately 0.13 per watt (visual factor efficiency) with photopic conversion of 89 lm/W. These figures correspond to an approximate wavelength of 483 nm.

$$\text{1 Watt at 483 nm} = \eta \times \text{1 W} \times \text{683 lm/W} = \text{89 lm}, \ \eta = 0.13$$
$$\text{200 Watt at 483 nm} = 0.13 \times \text{200 W} \times \text{683 lm/W} = \text{17800 lm}$$

Table 5.3 summarises the performance of the PV module within the enclosure of the solar simulator.

Table 5.3: PV module electrical performance within the enclosure of the solar simulator

Short circuit current I_{sc}	0.337A
Open Circuit Voltage V_{oc}	19.8V
Amount of light intensity	78 W/m^2
Light intensity	1/10 full Sun

5.3.4.3 Component Characteristics

5.3.4.3.1 KD70SX-1P PV Module Characteristics

The I - V and P - R characteristics of the PV module within the solar simulator enclosure at different LED floodlight luminous levels are tested using a power resistor box. The current and power output of the PV module are approximately proportional to the light intensity as shown in Figure 5.16 and Figure 5.17 respectively. At a given intensity, the solar module output current and voltage are determined by the load. The LED floodlight is set at different intensities to investigate the behaviour of the PV module within the enclosure. The LED floodlight is set at three different intensities: 78 W/m^2 (1/10 of the full sun, 6.7A LED forward current), 47.2 W/m^2 (1/20 of the full sun, 3.2A LED forward current) and 18.6 W/m^2 (1/50 of the full sun, 1A LED forward current). The maximum PV power with maximum LED floodlight is approximately 4.4 W.

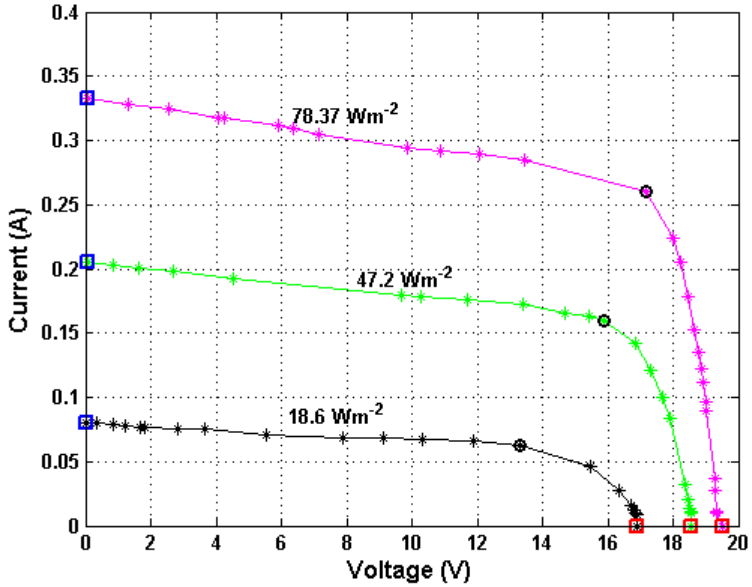

Figure 5.16: The experimental I-V curves of KD70SX-1P module at various solar simulator levels

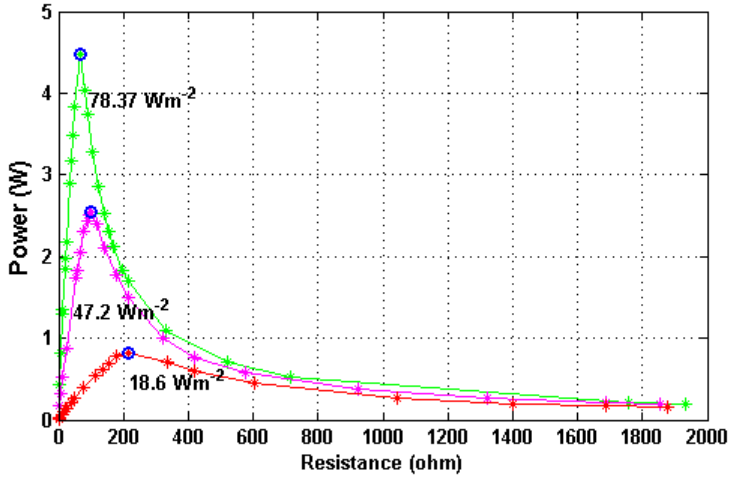

Figure 5.17: The experimental P-R curves of KD70SX-1P module at various solar simulator levels

The electrical characteristics of the PV module within the solar simulator enclosure at various insolation levels is summarized in Table 5.4.

Table 5.4: Electrical performance of individual cells and their series combinations

Electrical Performance	Solar Intensity		
	78.37 W/m^2	47.2 W/m^2	18.6 W/m^2
I_{sc}	337 mA	205 mA	80 mA
V_{oc}	19.8 V	18.55 V	17 V
V_{MPP}	17.19 V	15.87 V	13.29 V
I_{MPP}	260 mA	160 mA	62 mA
P_{MPP}	4.4 W	2.5 W	0.8 W
R_{opt}	66.1 ohm	99.1 ohm	214.3 ohm

5.3.4.3.2 200 W LED Floodlight (luminous flux of 17800)

The LED floodlight is tested using a bench power supply to investigate the relationship between the LED forward current and the PV module short circuit current as given in Figure 5.18.

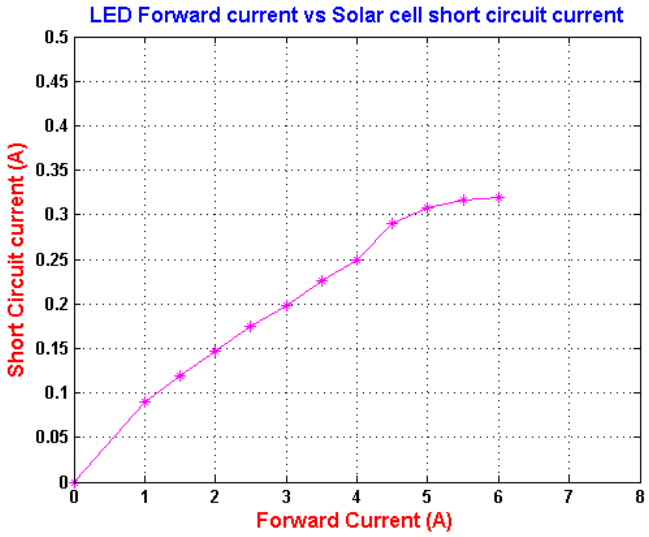

Figure 5.18: The LED forward current vs PV short circuit current

Figure 5.19 shows the relationship of the LED current and the percentage of LED floodlight intensity.

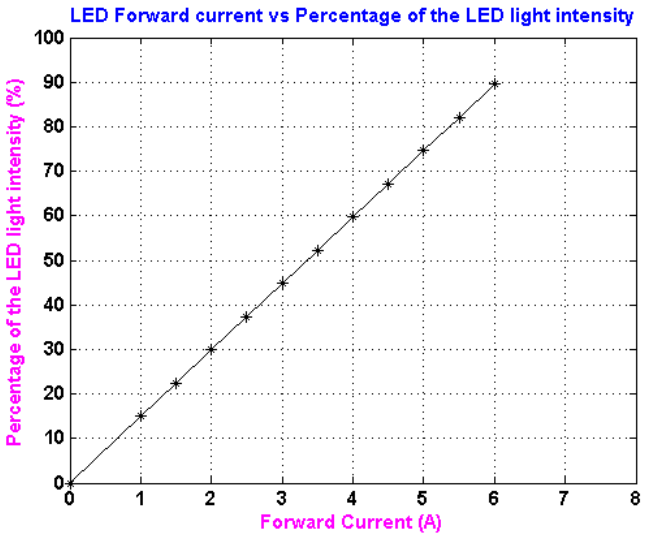

Figure 5.19: The LED forward current vs the percentage of light intensity

The figures clearly show that the PV performance is mainly dependent on the light intensity. The LED flood light in this study is controlled by the PC using the Mbed microcontroller to set the intensity of the solar simulator to any given intensity reference within the LED floodlight capability (78W/m^2 max). Beyond this an approximation procedure will be applied with ± errors.

5.3.4.3.3 Four-switch buck-boost converter

The power characteristics versus the duty cycle of the buck-boost converter incorporated with the solar simulator system at a resistive load of 1.2Ω is obtained at full luminous conditions as in Figure 5.20. The relationship of the ratio of the converter output voltage to the PV input voltage and the duty cycle of the converter is also found as illustrated in Figure 5.21. The equivalent resistance seen from the PV module versus the power is obtained and displayed in Figure 5.22.

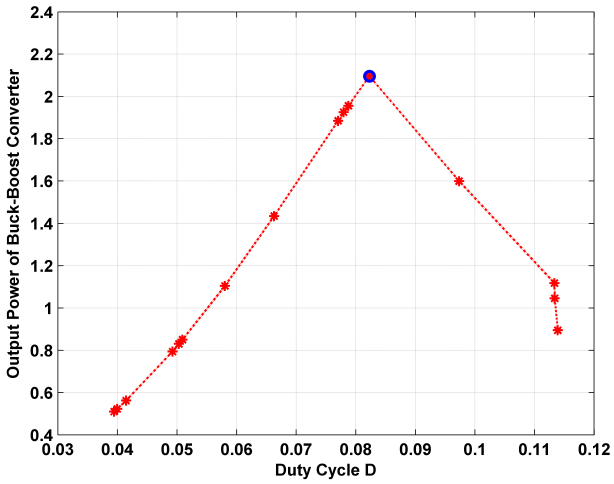

Figure 5.20: Experimental relationship between the output power of the buck-boost converter and the duty cycle at the maximum luminous condition of the solar solar simulator

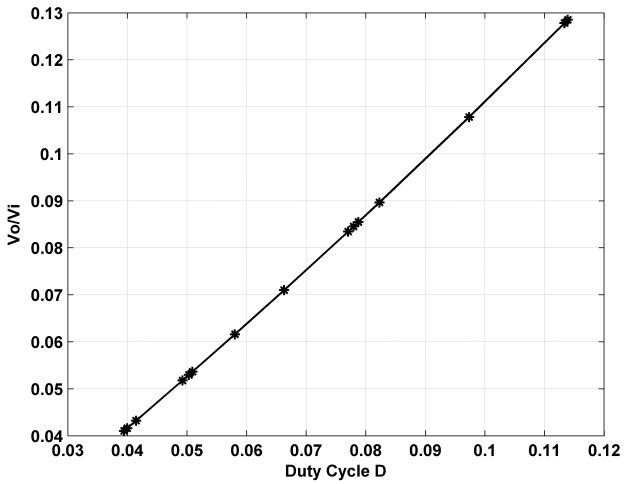

Figure 5.21: Experimental relationship between $\frac{V_o}{V_i}$ and the duty cycle of the buck-boost converter

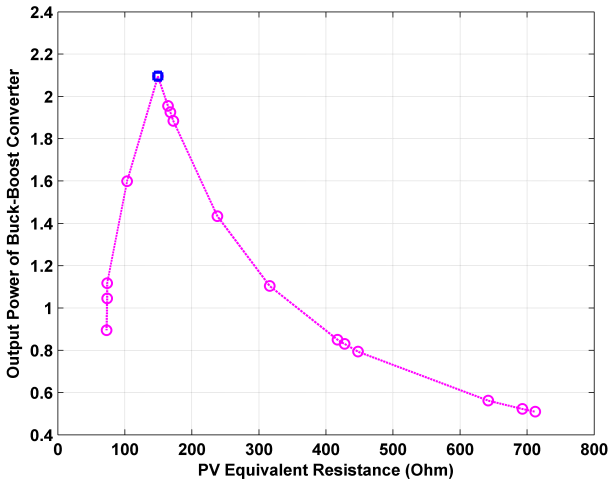

Figure 5.22: Experimental relationship between the output power of the buck-boost converter and the PV equivalent resistance at maximum luminous condition of the solar simulation

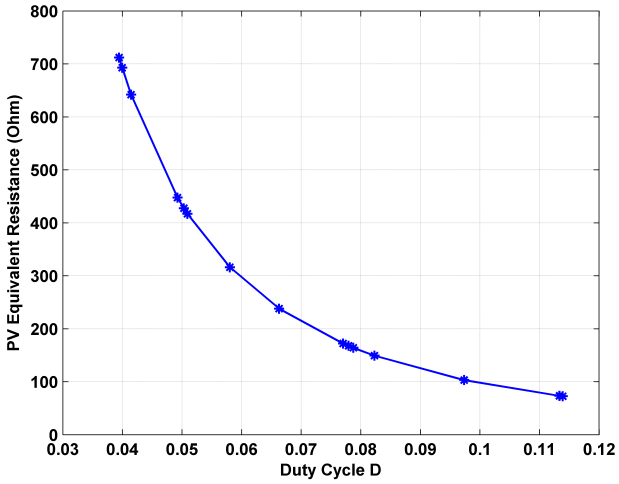

Figure 5.23: Experimental relationship between the PV equivalent resistance and duty cycle of the buck-boost converter

It is noticeable from Figure 5.23 that the PV equivalent resistance depends only on the buck-boost converter duty cycle D because of the fact that the equivalent resistance is proportional to the duty cycle as shown previously in equation 5.24. The maximum

output power of the buck-boost converter is achieved at a very small duty cycle.

5.3.5 Experimental and Simulation Results of MPPT Optimizer

5.3.5.1 Forward - Backward MPPT Algorithm Simulation

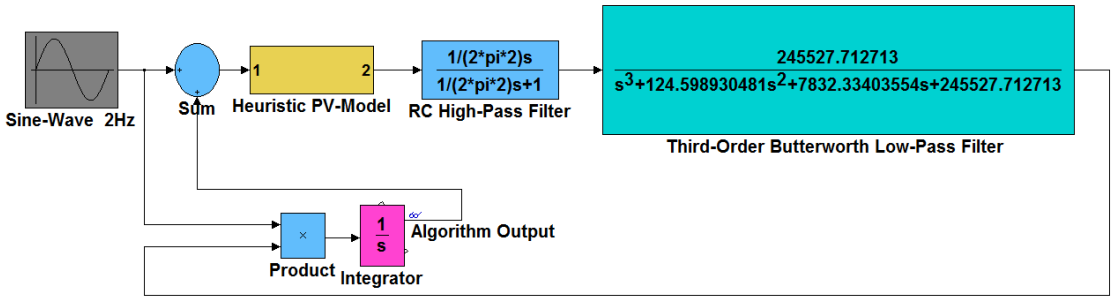

Figure 5.24: The Simulink simulation of the forward-backward MPPT algorithm

The Simulink simulation of the forward-backward algorithm is shown in Figure 5.24. The simulation of MPPT forward-backward algorithm requires a solar panel model, a high-pass filter block, a low-pass filter block and an integrator block. A heuristic PV model is, hence, modelled by a non-linear equation which represents a load R for quasi-short circuit current and $\frac{1}{R}$ for quasi-open circuit voltage as equation in (5.26).

$$P(\frac{R}{R_{max}}) = \frac{2P_{max}(\frac{R}{R_{max}})}{1 + (\frac{R}{R_{max}})^2} \tag{5.26}$$

where, R is the load, R_{max} is the optimum load, and P_{max} is the maximum power. Taking an experimental measured data of a PV module (KD70SX-1P) at 78 Wm^{-2}

light intensity to investigate the P-R characteristic of the heuristic PV equation. The latter is compared with the real P-R plot as in Figure 5.25.

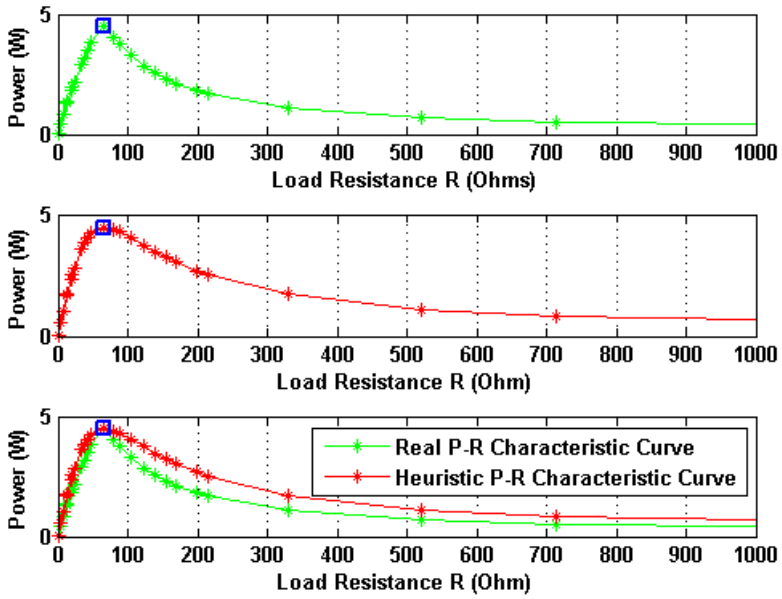

Figure 5.25: The real P-R curve and the heuristic P-R curve of the PV module (KD70SX-1P) are plotted using experimental data

As one can observe from the plots, the real P-R curve and the heuristic P-R curve have a similar trend and more importantly the MPP is located exactly at the same position.

$$P(u) = \frac{2u}{1+u^2} \tag{5.27}$$

Equation (5.27) shows the normalized version of equation (5.26), where $P_{max} = 1$ and $\frac{R}{R_{max}} = u$. The waveform characteristic of a sinusoidal input (u) to the non - linear equation at $u > 1$, $u < 1$ and $u = 1$ is illustrated in Figure 5.26. It is evident that the slope of the heuristic equation with a sinusoidal input is positive $\frac{R}{R_{max}} > 1$, while a negative slope is at $\frac{R}{R_{max}} < 1$, and no slope appears at $R = R_{max}$.

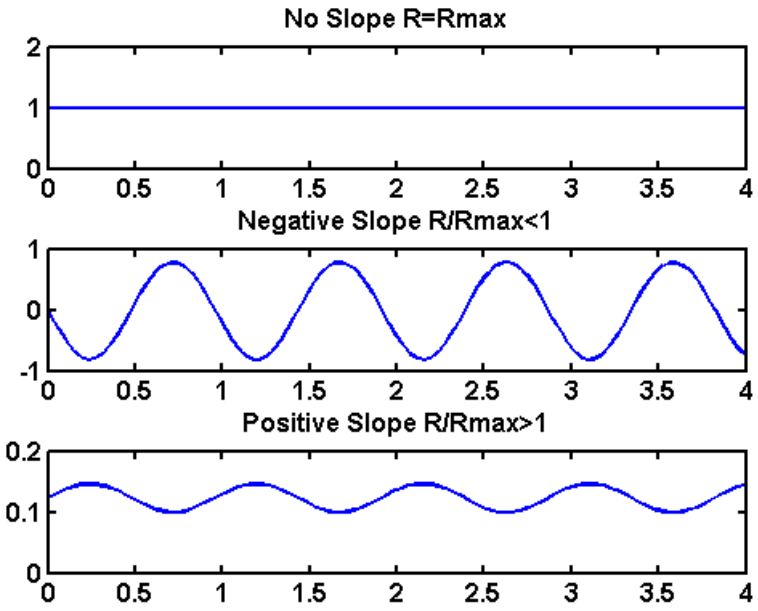

Figure 5.26: The relation between $P(u)$ and u in the heuristic model at different $\frac{R}{R_{max}}$ values

The Simulink subsystem implementation of the heuristic PV model is illustrated in Figure 5.27. The insolation reference here is set by the non - linear equation factor which is 2.

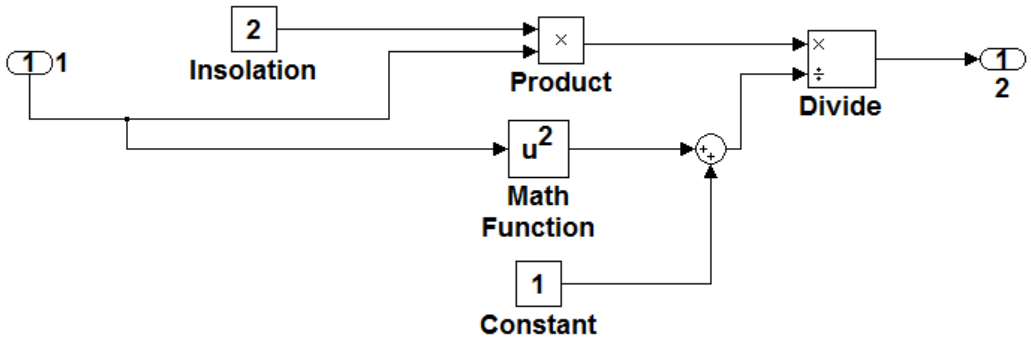

Figure 5.27: The Simulink layout of the heuristic PV model

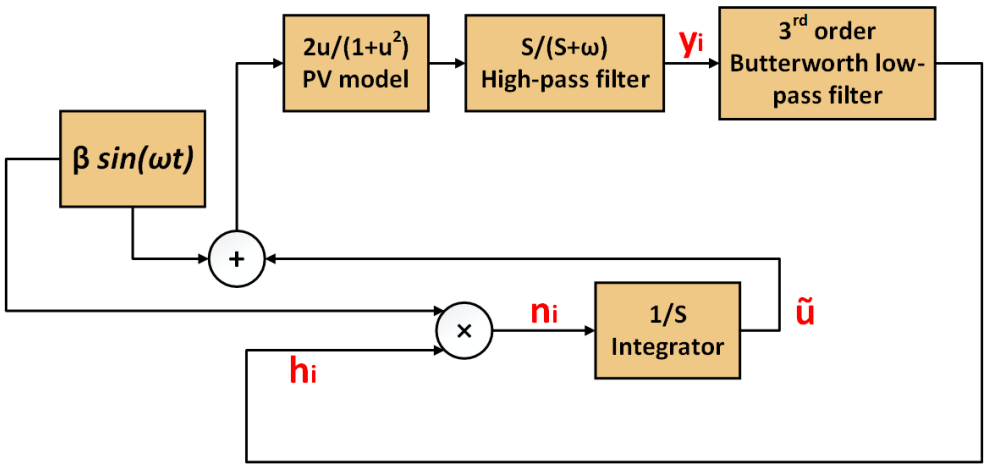

Figure 5.28: The block diagram of the simulated forward-backward MPPT algorithm

The simulation of the algorithm figure is redrawn as a block diagram as shown in Figure 5.28. The algorithm works by adding a 2 Hz periodic sinusoidal perturbation signal $\beta \sin(\omega t)$ to ũ the best estimate of u that maximizes the output power. The output of this passes through the normalized heuristic PV model to produce perturbations in the output power. A high-pass filter block at 2 Hz cut-off frequency approximates the DC component which is removed by applying a third order Butterworth low-pass filter (Sallen and Key design) of 10 Hz. The cascaded high-pass and low-pass filters creates a low quality factor Q, band-pass filter with a band range from 2 Hz to 10 Hz. The product of $\beta \sin(\omega t)$ and h_i creates approximately two sinusoidal signals n_i in which is being integrated (the gradient) and fed back to the system. This causes the control variable to track and find the MPP. The output signal is captured at ũ.

As discussed in Chapter 5 that the proposed technique tracks the MPP under rapidly varying irradiance conditions. The algorithm is, hence, tested under different insolation levels: reference level condition (insolation = 2), more irradiance level (Q_{More} =

5*insolation) and low insolation level (Q_{less} = 0.25*insolation).

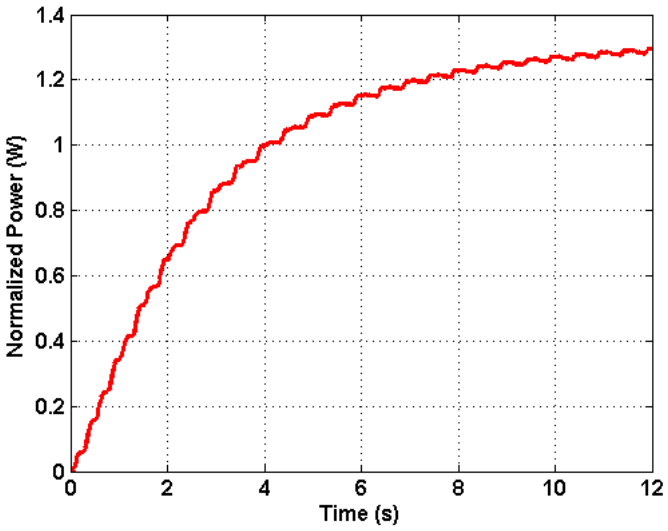

Figure 5.29: The performance of the forward - backward algorithm at the reference condition

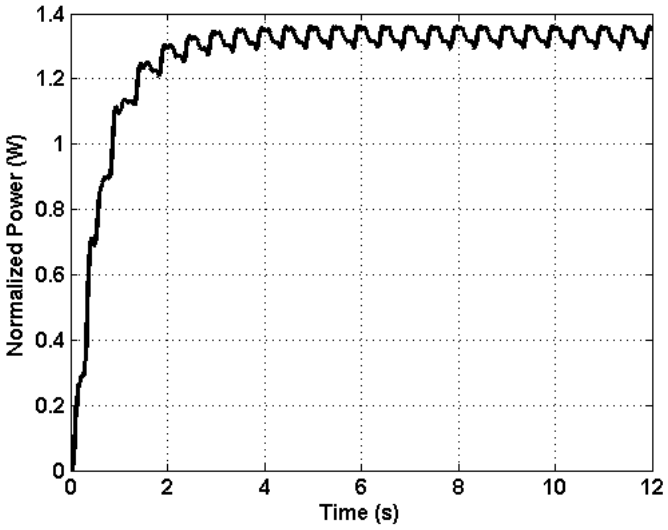

Figure 5.30: The performance of the forward - backward algorithm at Q_{More}

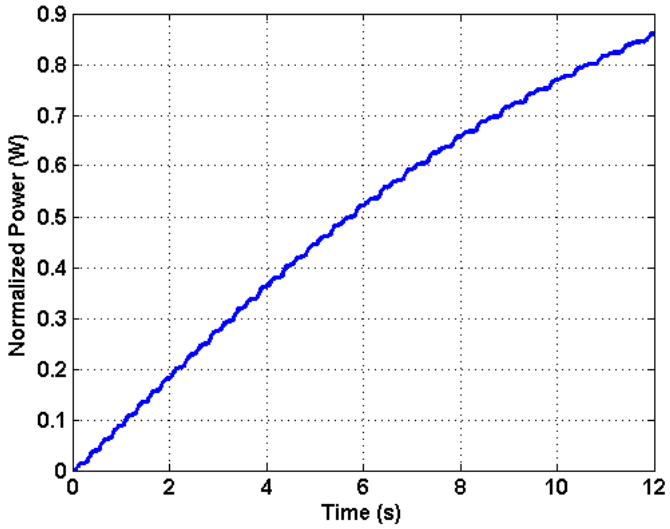

Figure 5.31: The performance of the forward - backward algorithm at Q_{less}

Figures 5.29, 5.30 and 5.31 demonstrate that the proposed algorithm can rapidly locate the MPP with guaranteed stability under varying insolation conditions. This is due to the fact that a PV panel is operating effectively in bright days (more insolation) as it receives the maximum amount of light possible. However, a PV panel works less effectively in cloudy days (less insolation). It is also shown that the MPP is rapidly located with the increased irradiance level as in Figure 5.29 and Figure 5.30 compared to Figure 5.31. However, the performance of the algorithm at low insolation is still successfully locating the MPP regardless of the speed. The forward-backward technique is clearly observable in the figures in particular Figure 5.30.

5.3.5.2 Load - Side, Forward - Backward MPP Optimizer Experimental Prototype

The experimental setup of the load-side, forward - backward optimizer is discussed in detail in the previous section. The off-the-shelf, DC to DC buck-boost converter is used in current mode by altering the duty cycle to maximize the current into the set load (1 Ω resistive). The load current is observed using a USB digital multimeter. The multiple-step, forward-backward algorithm is implemented in MATLAB to process the data and find the MPP (Code is included on a CD). The multiple step algorithm was initially tested under three insolation conditions which were achieved by setting the current of the LED-flood-light to 6.7A (maximum flux), 3A and 2A as illustrated in Figure 5.32. To highlight the algorithm, the forward steps after the MPP are illustrated in the curves for each insolation level.

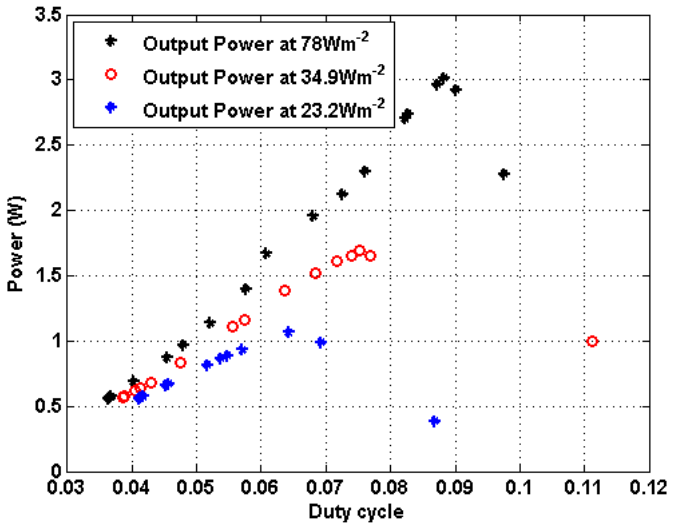

Figure 5.32: The experimental performance of the forward-backward algorithm at three insolation levels

The algorithm stops tracking when the maximum current and hence power are reached. The maximum current at each insolation level is therefore highlighted in Figure 5.33.

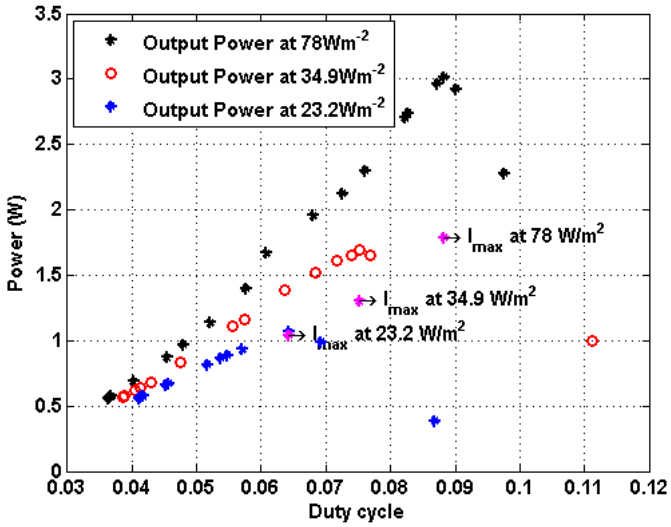

Figure 5.33: The maximization of power and current at three insolation levels

It is obvious from Figure 5.32 that the proposed algorithm is successfully locating the MPP at 3.1 W, 1.69 W and 1.06 W for 78 Wm^{-2}, 34.9 Wm^{-2} and 23.2 Wm^{-2} respectively. The current is maximized into the load as clearly marked in Figure 5.33. Approximately 1.2 W is being consumed by the buck - boost converter at the maximum insolation curve. Additionally, the converter is only operated in the buck mode due to the limitation in the generated power from the solar simulator which is approximately 4.3 W.

The algorithm is further validated by testing the position of the point on the curve (uphill, MPP and downhill) to ensure that the MPP does not get off-track with the change in the insolation level. The first test was a point climbing the hill at 23.2 Wm^{-2} insolation level with sudden rise in irradiance level to 78 Wm^{-2} and a point climbing a hill at the 78 Wm^{-2} curve with a sudden drop in the irradiance level to

23.2 Wm^{-2} as shown in Figure 5.34 and Figure 5.35, respectively.

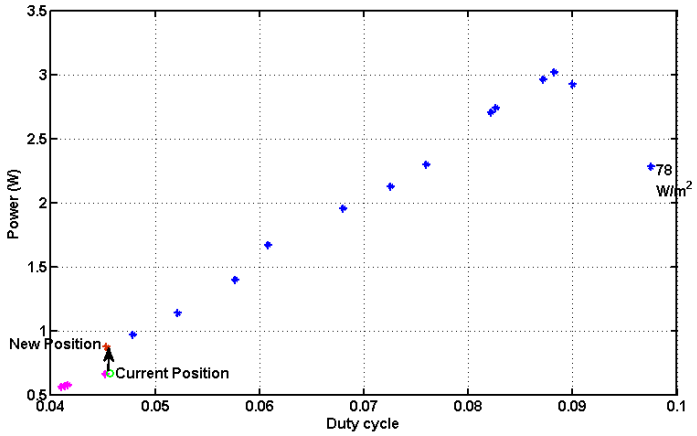

Figure 5.34: The current point is on an uphill position on 23.2 Wm^{-2} curve with a sudden rise in the insolation level to 78 Wm^{-2}

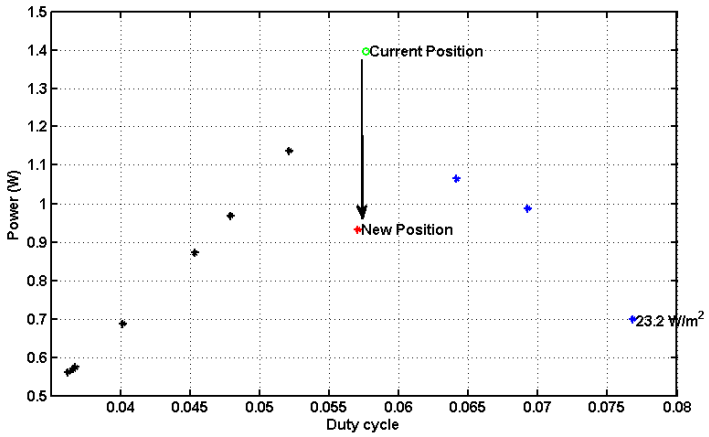

Figure 5.35: The current point is on an uphill position on 78 Wm^{-2} curve with a sudden drop in the insolation level to 23.2 Wm^{-2}

Secondly, the algorithm is evaluated at a point positioned on the downhill of 23.2 Wm^{-2} with a sudden increase in the irradiance level 78 Wm^{-2}, and a point positioned at the downhill curve of 34.9 $\frac{W}{m^2}$ with sudden drop in irradiance level to 23.2 Wm^{-2} as shown in Figure 5.36 and Figure 5.37 respectively. Finally, the algorithm is further

checked at MPP with a sudden rise and drop in the insolation level as shown in Figure 5.38 and Figure 5.39.

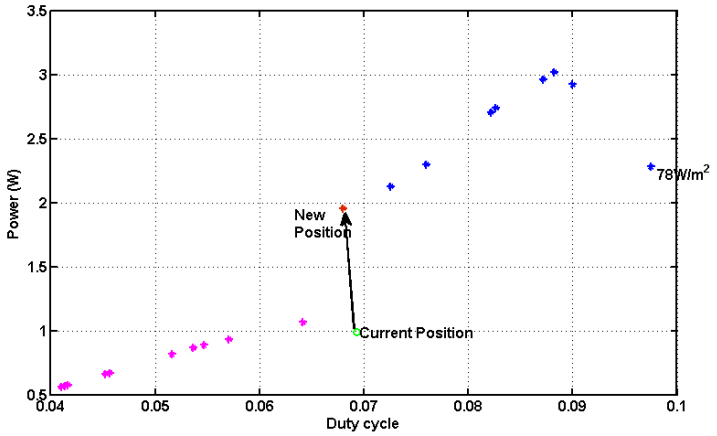

Figure 5.36: The current point is on a downhill position on 23.2 Wm^{-2} curve with a sudden rise in the insolation level to 78 Wm^{-2}

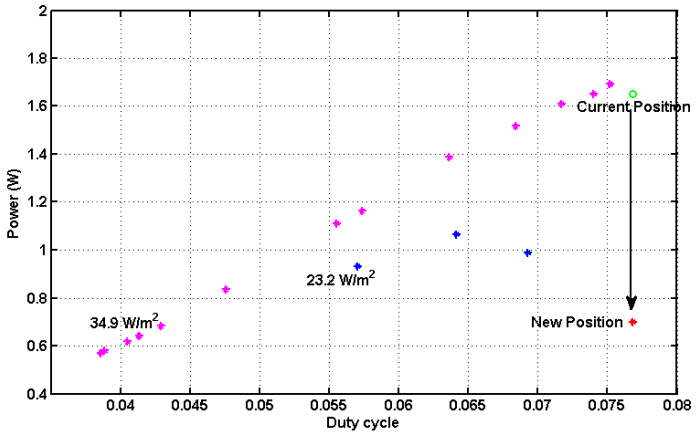

Figure 5.37: The current point is on a downhill position on 34.9 Wm^{-2} curve with a sudden drop in the insolation level to 23.2 Wm^{-2}

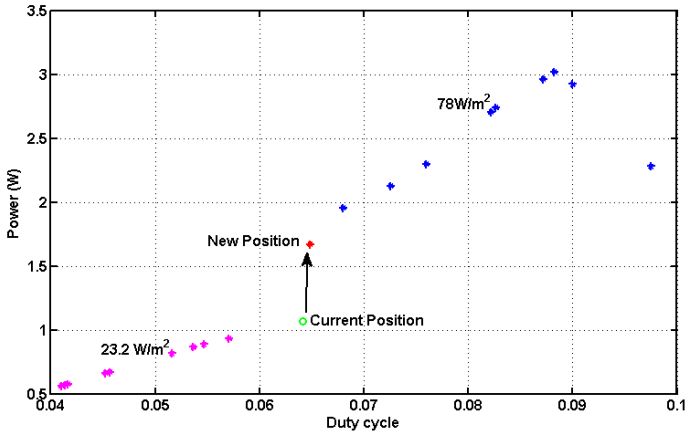

Figure 5.38: The current point is located at the MPP on 23.2 Wm^{-2} curve with a sudden rise in the insolation level to 78 Wm^{-2}

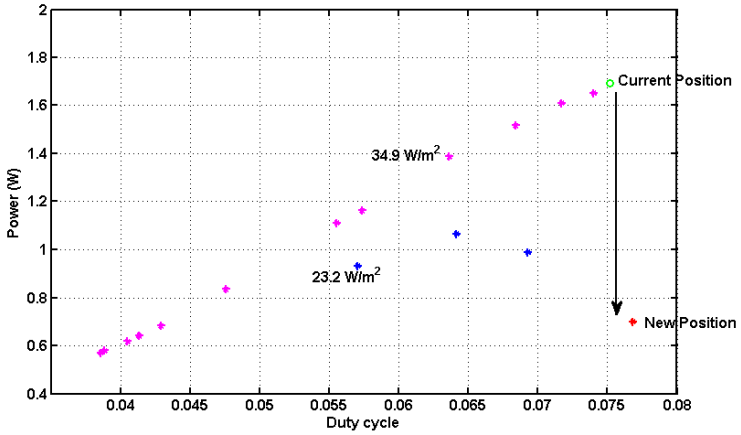

Figure 5.39: The current point is located at the MPP on 34.9 Wm^{-2} curve with a sudden drop in the insolation level to 23.2 Wm^{-2}

The forward multiple points in Figure 5.34, Figure 5.35, Figure 5.36 and Figure 5.38 are highlighted to clearly show the validation of the proposed algorithm. In Figure 5.37 and Figure 5.39, a backward point is highlighted as the proposed algorithm climbing the downhill curve to accurately find the MPP. The experimental results here give strong evidence that the proposed MPPT system successfully finds the

MPP at rapidly varying irradiance conditions.

5.4 Conclusion

In this chapter, a new mathematical method to determine the timing steps of multi-level signal of known amplitude has been presented. The optimization method presented is not confined to known amplitude signals; it can be also applied to unknown amplitude signals for given time steps.

A load-side, maximum power point tracking based on multiple step, forward-backward algorithm with direct control has also been discussed in this chapter. The MPPT technique presented here guarantees tracking the maximum power point under various weather conditions and operates at unity power factor.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Summary and Conclusions

Circuit complexity and power dissipation are an issue of major concern in ever growing PV inverters. Low efficiency is an increasing problem with the growth of solar power systems. Hence, there is a need to design inverters with the maximum efficiency and least circuit complexity. The work described in this thesis was aimed at addressing these problems in low power applications. This has been achieved by developing prototypes of two DC-to-AC, multilevel PV inverters and presenting experimental and simulation results. The task of determining the timing steps of multilevel signals

of known amplitude is resolved using a completely new mathematical method. A significant task in the solar MPPT design is understanding the necessary trade-offs in terms of circuit characteristics and acceptable efficiency levels, in order to achieve the identified target system performance. In that aspect, a load-side, multiple step, forward-backward MPPT algorithm is proposed to potentially have a crucial role in maximizing the power into a given load.

The first DC-to-AC multilevel inverter for PV application described in Chapter 3 is based on Golomb ruler cell voltage selection which allows individual panel outputs to be aggregated in an optimal fashion to produce a low-distortion, approximate sine-wave signal. This gives a direct conversion with a low frequency switching and a non-linear, step size, DC-to-AC multilevel based on two ladders of switches structured as the Golomb ruler. The expressions for both series resistance and switching losses are derived and evaluated numerically. A MATLAB based program has been developed for optimal Golomb rulers with a user-friendly interface to determine the deficiency for a given order. The Golomb technique is not proven to be as efficient as a conventional pure sine-wave inverter due to unevenly utilized PV sources. The latter makes Golomb topology less preferable. The experimental and simulation results for the third-order Golomb direct conversion scheme using low-power PV modules are presented in Chapter 3 which demonstrates the capability and the validity of the technique.

The six-level, DC-to-AC, staircase Golomb inverter is further simulated in Simulink, which required switching controller to control the MOSFET switches according to the Golomb switching control scheme. The simulation results confirm the efficacy of

the technique for PV application with only six voltage output levels. The THD of the output signal is approximately 16.14% (-15.8 dB) and the third harmonic magnitude percentage of the fundamental is 0.5%. It is difficult to set the time duration of the DC voltage levels to the exact required duration due to the Simulink package limitation.

The laboratory implementation of the third-order Golomb inverter required a microcontroller. Mbed NXP LPC1768 microcontroller is used to control the bidirectional switches and generate the periodic digital pulses at the specified DigitalOut pins. Besides, a heuristic technique is used to determine the timing steps of the output levels which are set in the main program of the microcontroller. The experimental output signal shows a close correlation with the simulated results in terms of the generated voltage levels. However, the total harmonic distortion is slightly different from the simulated results. This differs because of the fact that the timing steps in the experiment are not the same as in the simulation.

The second DC-to-AC multilevel inverter for PV application explained in Chapter 4 is based on a cyclic voltage selection technique which ensures complete panel utilization and produce a good-quality, sine-wave output signal. The need for magnetic materials is removed by selecting series and parallel combinations of PV cells. This technique allows on-panel battery provision such that a complete generation and storage module is realized. The cyclic inverter with batteries is proven mathematically to be as efficient as a conventional magnetic core-based inverter with storage. A mathematical model of the cyclic selection algorithm is first derived and the numerical evaluation is obtained using MATLAB that gives a user-friendly interface to the model. Expressions for the switching losses and the optimum number of MOSFETs within a cyclic

level circuit are derived.

Experimentally, the inverter was implemented using solar powered, lithium-ion batteries based on the third order cyclic selection algorithm to generated 7-levels, voltage output signal. Mbed NXP LPC 1768 microcontroller is employed to control the photo-switches and generate periodic digital output waveforms at the specified DigitalOut pins. The timing steps are determined using the proposed optimization method (Chapter 5) and set in the main program of the microcontroller. The experimental inverter produced excellent results with 7 voltage-level stages. The FFT of the experimental output showed a 33.5 dB difference between the fundamental and third harmonics at 150 Hz exhibiting the expected harmonic reduction in the 7-level inverter. Simulink simulations further validate the 7-level cyclic inverter by giving 13.64% THD.

A new mathematical method for determining the timing steps of the multilevel signal of a known amplitude is derived and evaluated numerically in MATLAB which is presented in Chapter 5. The proposed timing steps method gives the same results as the well-known Fourier series method but requires no carefully-chosen optimization starting point. Additionally, this method is real-time adaptive and can be used for an unlimited number of levels. This latter feature is beyond the reach of computationally-intensive Fourier methods. Experimental evaluation of the optimization method is performed in the cyclic inverter to show the effectiveness of the technique over the equal timing steps method. The third harmonic of the cyclic inverter using the optimized method is approximately 2% of the fundamental while it is about 14.1% in the equal timing steps method.

In Chapter 5, second order central difference theory is employed to evaluate the multiple step MPPT algorithm regime for a load-side optimization. The forward-backward difference algorithm is then simulated in Simulink by using a heuristic PV model. This model is proven mathematically and numerically to have the same characteristic as a real PV module. Simulation results show that the proposed algorithm successfully tracks the MPP at various irradiance conditions.

Experimentally, the MPPT optimizer was implemented using a controllable, indoor, solar simulator and an off-the-shelf, four-switch, DC-to-DC buck boost converter. The data of the solar simulator for three different irradiance levels are processed in MATLAB. Also a MATLAB based program has been developed for the proposed MPPT that gives a user-friendly interface. The experimental results validate the algorithm under different weather conditions and the location of the MPP on the curve.

It is hoped that the proposed multilevel topologies along with the optimization methods in this thesis will prove valuable in improving the PV conversion efficiency.

6.2 Suggestions for Future Work

Several aspects of the Golomb ruler inverter have been examined for single phase, low power applications. Nevertheless, most of the analysis presented can be applied to three phase high power applications. The three phase analysis has not been carried out. Essentially, the analysis to be used requires firstly a proper choice of the Golomb ruler order. The three phase technique requires some form of storage to overcome

the redundancy in the DC sources and thus ensure they are evenly utilized. In other words, when the source is not utilized, it can be used to charge a capacitor or a battery and in turn contributes in one of the other phases.

The third-order Golomb ruler is used here to realize the proposed inverter and synthesize a near sinusoidal output signal. For the experimental and simulation results, only 6 levels are generated, however, this can be increased by using higher order Golomb rulers.

The investigation of the use of Golomb ruler is directly applicable to tap changers. As a result, an immediate expansion of the present work is to switch the PV source through a tap changer which is placed such as a Golomb ruler is realized. The required levels could thus be generated to produce a good quality sine-wave output signal.

The solar shading problems have not been tackled in either of the multilevel inverters here. The Golomb inverter has the option of panel blocking in the event of shading. An investigation of the shading effect needs to be carried out experimentally. The cyclic inverter circumvents the solar shading problem by shuffling the shaded cell. This is another important extension to the cyclic inverter and thus an investigation in that direction has to be assessed by experimental and simulation studies.

Based on the expression of the optimum number of MOSFETs derived in Chapter 4, it is possible to proceed in producing the corresponding multilevel output signal for a given maximum voltage and current of PV panels.

Another important extension of the analysis of the timing steps optimization in Chapter 5 would be its application in real-time. An interesting matter would be reading

both the selected and the maximum voltages by the microcontroller in real-time. The main motive behind this is enabling the accuracy of the optimization method and thus minimizes the harmonic distortion in the output signal.

Then, a very important research area would be the investigation of the load-side MPPT using multiple-step, forward-backward algorithm in AC load. More specifically, the load-side MPPT can be applied at the AC output of a multilevel inverter to maximize the current into any given load through a possible AC to AC buck converter. Finally, a complete generation and storage multilevel cyclic inverter with MPPT and shading observer need to be implemented and investigated as a one unit.

An interesting addition in the Golomb and cyclic selection inverters would be to include a MPPT control system as both can not find the MPP automatically.

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Appendices

APPENDIX A

C++ COMPILER CODES

A.1 C++ Online Compiler Program for Multilevel Golomb Inverter

This is C++ implementation of 6 - level Golomb inverter.

```
#include "mbed.h"
DigitalOut MOS1(p17);
DigitalOut MOS2(p18);
DigitalOut MOS3(p15);
```

```
DigitalOut MOS4(p19);
DigitalOut MOS5(p16);
DigitalOut MOS6(p20);
Timer t;
int main() {
t.start();// This starts the timer
while (1) {
if (t.read()>=0.0 && t.read() <= 0.0016) {
// First step in the positive half cycle
MOS1 = 1;
MOS2 = 0;
MOS3 = 0;
MOS4 = 1;
MOS5 = 0;
MOS6 = 0;     }
if (t.read()>0.0015 && t.read()<=0.0032) {
MOS1= 0;
MOS2= 0;
MOS3= 1;
MOS4= 0;
MOS5= 0;
MOS6= 1;       }
if (t.read()>0.0032 && t.read()<=0.0068) {
MOS1= 1;
```

```
MOS2= 0;
MOS3= 0;
MOS4= 0;
MOS5= 0;
MOS6= 1;          }
if (t.read()>0.0068 && t.read()<= 0.0085) {
MOS1= 0;
MOS2= 0;
MOS3= 1;
MOS4= 0;
MOS5= 0;
MOS6= 1;          }
if (t.read ()>0.0085 && t.read ()<=0.01) {
MOS1=1;
MOS2=0;
MOS3=0;
MOS4=1;
MOS5=0;
MOS6=0;           }
if (t.read ()>0.01 && t.read() <= 0.0116) {
// This the first step in the negative half cycle
MOS1=0;
MOS2=1;
MOS3=1;
```

```
MOS4=0;
MOS5=0;
MOS6=0;          }
if (t.read ()>0.0115 && t.read ()<=0.0132) {
MOS1=0;
MOS2=0;
MOS3=0;
MOS4=1;
MOS5=1;
MOS6=0;          }
if ( t.read ()>0.0132 && t.read () <=0.0168) {
MOS1=0;
MOS2=1;
MOS3=0;
MOS4=0;
MOS5=1;
MOS6=0;          }
if ( t.read() >0.0168 && t.read ()<=0.0185) {
MOS1=0;
MOS2=0;
MOS5=1;
MOS4=1;
MOS3=0;
MOS6=0;          }
```

```
if (t.read() >0.0185 && t.read ()<= 0.02) {
MOS1=0;
MOS2=1;
MOS3=1;
MOS4=0;
MOS5=0;
MOS6=0;          }
if (t.read() > 0.02) {
t.reset();          }      }    }
//This resets the timer
```

A.2 C++ Online Compiler Program for Multilevel Cyclic Selection Multilevel Inverter

This is C++ implementation of 7 - level cyclic selection Inverter.

```
#include "mbed.h"
Timer t;
DigitalOut myled(p21);
DigitalOut myled1(p22);
DigitalOut myled2(p23);
DigitalOut myled3(p24);
int main() {
t.start();
```

```
while(1) {
//************************************//
//Positive
if (t.read()>=0.0 && t.read() <= 0.00052) {
myled=0;
myled1=0;
myled3=0;
myled2=0; }
if (t.read()> 0.00052 && t.read()<=0.00168) {
myled=0;
myled1=0;
myled3=1;
myled2=0;}
if (t.read()>=0.00168 && t.read() <=0.00242) {
myled=1;
myled1=0;
myled3=1;
myled2=0;  }
if (t.read()>=0.00242 && t.read() <=0.00316) {
myled=0;
myled1=1;
myled3=1;
myled2=0;  }
if (t.read()> 0.00316 && t.read()<=0.005) {
```

```
myled=1;
myled1=1;
myled3=1;
myled2=0;   }
if (t.read()>0.005 && t.read() <= 0.00684) {
myled=1;
myled1=1;
myled3=1;
myled2=0; }
if (t.read()>0.00684 && t.read() <= 0.00758) {
myled=1;
myled1=0;
myled3=1;
myled2=0; }
if (t.read()>0.00758 && t.read() <= 0.00832) {
myled=1;
myled1=0;
myled3=1;
myled2=0; }
if (t.read()>=0.00832 && t.read() <= 0.00948) {
myled=0;
myled1=0;
myled3=1;
myled2=0; }
```

```
if (t.read()> 0.00948 && t.read()<=0.01052) {
myled=0;
myled1=0;
myled3=0;
myled2=0;}
//*****************************************//
//Negative
if (t.read()> 0.01052 && t.read()<=0.01168) {
myled=0;
myled1=0;
myled3=0;
myled2=1;  }
if (t.read()>0.01168 && t.read() <=0.01242) {
myled=1;
myled1=0;
myled3=0;
myled2=1; }
if (t.read()>0.01242 && t.read() <=0.01316) {
myled=0;
myled1=1;
myled3=0;
myled2=1; }
if (t.read()>0.01316 && t.read() <= 0.015) {
myled=1;
```

```
myled1=1;
myled3=0;
myled2=1; }
if (t.read()>0.015 && t.read() <= 0.01684) {
myled=1;
myled1=1;
myled3=0;
myled2=1; }
if (t.read()>0.01684 && t.read() <= 0.01758) {
myled=1;
myled1=0;
myled3=0;
myled2=1; }
if (t.read()>0.01758 && t.read() <= 0.01832) {
myled=0;
myled1=1;
myled3=0;
myled2=1; }
if (t.read()>0.01832 && t.read() <= 0.01948) {
myled=0;
myled1=0;
myled3=0;
myled2=1; }
if (t.read()>0.01948&& t.read() <= 0.02){
```

```
myled=0;
myled1=0;
myled3=0;
myled2=0; }
if (t.read() > 0.02) {
t.reset();
}}
}
```

APPENDIX B

LIST OF PUBLICATIONS & SEMINARS

1. N. M. Ramli, and S.D. Walker, First Realisation of a Golomb Ruler Staircase Inverter for Photovoltaic Applications IEEE 5th Computer Science and Electronic Engineering Conference (CEEC) 2013

2. Golomb Ruler-Based Switched - Rail Photovoltaic Power Optimiser, Seminar Imperial College London (19 March 2013)

3. Ramli, Naseem M., Salma AS Alarefi, and Stuart D. Walker. "Renewable power and microgeneration in Libya: Photovoltaic system sizing, wind, rainfall potentials and public response." Renewable Energy Congress (IREC), 2015 6th

International. IEEE, 2015.

4. Ramli, Naseem, and Stuart Walker. "Pan-global, annualized determination of solar collector optimum tilt angle." 2015 7th International Conference on Modelling, Identification and Control (ICMIC). IEEE, 2015.

5. Ramli, Naseem, and Stuart Walker. "Power maximization using multiple step, load-side, current-mode sensing." 2015 3rd International Renewable and Sustainable Energy Conference (IRSEC). IEEE, 2015.

6. Domoney, W. Frank, Naseem Ramli, Salma Alarefi, and Stuart D. Walker. "Smart city solutions to water management using self-powered, low-cost, water sensors and apache spark data aggregation." In 2015 3rd International Renewable and Sustainable Energy Conference (IRSEC), pp. 1-4. IEEE, 2015.

7. Cyclic Selection Lithium -Ion Battery Multilevel Inverter for Low Power Applications.(Selected Poster to showcase at the house of commons) (London March 2016)

8. Modelling and Simulation of Cyclic Selection Solar-Powered Lithium Ion-Battery Multilevel Inverter For Low power Applications (To be submitted to IEEE Transactions on Sustainable Energy)