

Extreme Total Ionizing Dose Survival of a COTS Artix-7 FPGA Under Prolonged Gamma Irradiation

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Abstract—Commercial Off-The-Shelf (COTS) FPGAs offer a low-cost platform for nuclear robotics, yet their radiation survivability is often underestimated because vulnerable onboard peripherals fail before the FPGA silicon. Furthermore, most studies irradiate unpowered devices at high dose rates, leaving Enhanced Low Dose Rate Sensitivity (ELDRS) behavior largely unexplored for these architectures. This paper presents an extended gamma irradiation campaign at Harwell, UK, where a Trenz Electronic TE0725 board hosting an AMD Artix-7 FPGA was continuously powered and actively benchmarked via 14 m of remote cables for 93.6 hours, accumulating a Total Ionizing Dose (TID) of 6,680 Gy $\pm 10\%$. Post-irradiation diagnostics confirmed that the Artix-7 silicon fabric remained functional and reprogrammable via JTAG, with stable internal voltage and temperature readings; only the QSPI flash memory failed, preventing autonomous reconfiguration. This work represents one of the longest continuously powered COTS FPGA irradiation campaigns in the literature, demonstrating survival beyond the ≈ 6.7 kGy threshold without local shielding, differentiating this work from previous lead-shielded architectures. The findings validate remote power delivery as a practical, cost-effective strategy for deploying COTS FPGAs in high-radiation environments.

Index Terms—Artix-7, COTS FPGA, ELDRS, Gamma Irradiation, Nuclear Robotics, Radiation Hardness, Remote Power Delivery, Total Ionizing Dose

I. INTRODUCTION

Autonomous robotic systems operating in nuclear environments must process sensor data, execute control algorithms, and maintain communication links while exposed to sustained gamma radiation. The AMD Artix-7 FPGA family, particularly the low-cost Commercial Off-The-Shelf (COTS) XC7A15T and XC7A35T variants, has attracted growing interest for these applications owing to its computational density, hardware reconfigurability, and competitive price point [1], [2].

A persistent limitation in characterizing the radiation resilience of such platforms is that standard COTS development boards carry onboard PMICs and USB-to-UART (FTDI) bridge controllers whose Total Ionizing Dose (TID) failure thresholds are far lower than those of the FPGA silicon itself. When these peripherals fail, the resulting power-rail collapse or communication loss is often misattributed to the FPGA fabric, significantly underestimating the true silicon tolerance [3], [4]. Physically removing local voltage regulators and supplying the FPGA from a remote, radiation-shielded

power network has been identified as an effective strategy to expose the intrinsic resilience of the silicon [4], [5].

A further gap in the existing literature concerns dose rate. The majority of published TID studies on COTS FPGAs employ high dose rates (typically 5–30 Gy/min, and sometimes exceeding 100 Gy/min in highly accelerated campaigns) for practical time constraints, leaving the dose-rate-dependent behavior of 28-nm COTS FPGAs inadequately characterized [6], [7]. Accelerated campaigns may not reflect real-world environmental conditions, and at the opposite extreme, very low dose rates can trigger Enhanced Low Dose Rate Sensitivity (ELDRS) where damage per unit dose is paradoxically enhanced in bipolar-sensitive oxide structures [8], effects whose magnitude in modern CMOS FPGAs remains underexplored. Despite its relevance to nuclear decommissioning, where operational dose rates are typically in the $\mu\text{Gy/min}$ to mGy/min range, ELDRS characterization of 28-nm COTS FPGAs remains unreported in the literature.

This paper addresses both gaps by reporting a 93.6-hour, near-continuous ^{60}Co irradiation of a remotely powered TE0725 board at Amentum’s Harwell facility, reaching a cumulative TID of 6,680 Gy at a dose rate of 1.2 Gy/min. The device was actively executing a multi-core computational benchmark throughout, and post-irradiation JTAG and XADC diagnostics confirm the silicon fabric is functional. The primary contributions of this work are three-fold: 1) providing a rare, system-level characterization of a 28-nm COTS FPGA during a continuous 93.6-hour campaign at an ELDRS-relevant dose rate; 2) validating that an unshielded 14 m remote Power Delivery Network (PDN) successfully bypasses local PMIC bottlenecks; and 3) conducting post-irradiation diagnostics that confirm the core fabric’s complete survival up to 6,680 Gy. Detailed parametric trends analysis is reserved for an upcoming journal expansion.

The rest of this paper is organized as follows: Section II reviews the background on TID effects, ELDRS, and peripheral vulnerabilities in COTS platforms. Section III outlines the experimental methodology, detailing the Device Under Test (DUT), the 14 m remote PDN, and the telemetry logging configuration. In Section IV, we present the experimental observations, including peripheral failure thresholds and post-

irradiation JTAG diagnostics. Section V contextualizes these findings against prior literature. Finally, Section VI concludes the paper and outlines directions for future research.

II. BACKGROUND AND RELATED WORK

A. TID Effects and ELDRS in COTS FPGAs

TID effects in MOS-based FPGAs are observed as charge accumulation in gate and field oxide layers, shifting transistor threshold voltages, increasing sub-threshold leakage currents, and ultimately causing functional collapse [6]. The severity of these effects depends not only on cumulative dose but also on dose rate. At moderately low rates, thermally activated annealing of oxide-trapped charge competes with charge buildup, often yielding an apparently higher effective failure threshold [6], [7]. At very low rates representative of real nuclear environments, however, devices may exhibit ELDRS (a phenomenon predominantly observed in bipolar-process structures) where reduced dose rates paradoxically increase damage per unit dose due to enhanced hole transport and trapping in sensitive oxide interfaces [8]. For 28-nm CMOS FPGAs, the dose-rate dependence across these regimes remains incompletely characterized, motivating the long-duration, low-dose-rate campaign reported here.

Studies on SRAM-based COTS FPGAs have reported this dose-rate dependence directly. For example, Gao et al. [7] showed that an SRAM-based FPGA failed at ≈ 2.1 kGy under a high dose rate yet remained functional at 2.5 kGy under a low dose rate, attributing the difference to slow oxide-charge generation allowing annealing to dominate. Similarly, Liu et al. [6] demonstrated that reducing the ^{60}Co dose rate from 171 to 2.68 mGy(Si)/s roughly doubled the failure threshold of an anti-fuse FPGA, which is consistent with an annealing-dominated mechanism. For 28-nm technologies specifically, the thin gate oxide that provides inherent TID resilience at high dose rates may interact with ELDRS differently from older process nodes, yet targeted low-rate campaigns on 28-nm COTS FPGA platforms (as opposed to isolated test structures) are rare.

B. Peripheral Vulnerability and Remote Power Strategies

A recurring finding across COTS board-level irradiation studies is that onboard power management circuitry fails well before the programmable logic fabric. West et al. [3] reported that a COTS single-board computer failed at a mean dose of 111 Gy that is linked to onboard power management faults, and suggested that power subsystem redesign could substantially extend operational life. Moreover, Fried et al. [4] demonstrated directly that replacing the onboard voltage regulator with an external shielded equivalent extended the survivable dose of a COTS microcontroller board to ≈ 350 Gy. Similarly, Nancekievill et al. [5] routed power and measurement lines through an irradiator feedthrough using a ribbon cable. This configuration enabled continuous monitoring while safely isolating sensitive control electronic chips outside the radiation zone.

These results collectively motivate the remote PDN approach adopted in this work. Notably, the majority of the studies above operated at high dose rates and short durations; none combined remote PDN with >6 kGy cumulative dose and 93.6 hours continuous active operation.

C. Artix-7 TID Survivability in Context

Published data on the Artix-7 and comparable 28-nm COTS FPGA platforms span a wide range of conditions. Bricas et al. [9] irradiated AMD Artix-7 (among other families) and reported no functional failure up to ≈ 3.1 kGy using an X-ray source with embedded propagation delay monitoring. Vartanian et al. [10] irradiated an AMD Kintex UltraScale evaluation board under active dynamic operation with ^{60}Co and observed no functional failure up to 6.2 kGy, with leakage currents recovering through annealing. Most directly comparable to this work, Hu et al. [11] conducted a ^{60}Co irradiation of Artix-7 platforms (28-nm) with lead shielding applied to onboard LDOs, reaching ≈ 6 kGy (silicon) before system-level failure, and reported JTAG chain and fabric integrity up to that dose.

The present study extends beyond this threshold to 6,680 Gy without local shielding of the FPGA board, instead relying on a remote 14 m PDN, and does so at a dose rate approximately one order of magnitude lower than typical high-rate ^{60}Co campaigns, thus making it relevant to directly assessing ELDRS behavior in a system-level context.

III. EXPERIMENTAL SETUP

A. Device Under Test

The DUT was a Trenz Electronic TE0725-04-21C-1-A carrier board hosting an AMD XC7A15T Artix-7 FPGA (28-nm HPL process). Prior to irradiation, the onboard power management components (specifically the MPM3834, MPM3860, TPS73025, and TPS3106K33 ICs) were physically removed to isolate the FPGA silicon from local voltage regulation entirely. The externally supplied rails were the core voltage V_{CCINT} (1.0 V), the auxiliary voltage V_{CCAUX} (1.8 V), and two I/O supply domains V_{CCIO} (2.5 V and 3.3 V). No local shielding was applied to the FPGA board or any of its remaining peripheral components.

The DUT was programmed with a Triple-Core MicroBlaze benchmark bitstream that continuously executed random integer matrix multiplications, monitored BRAM integrity, queried on-chip XADC sensors, and reported health telemetry via UART, which kept the device in full active operation throughout irradiation. Further details of the logging methodology are found in our prior work, which is yet to be published (under review) [12].

B. Remote Power Delivery Network

A custom remote PDN supplied all FPGA power rails from outside the irradiation chamber via 14 m of 18 AWG copper-aluminium composite cabling with silicone insulation, with the regulator circuits fabricated externally using similar IC topologies to the original board design (MPM and TPS

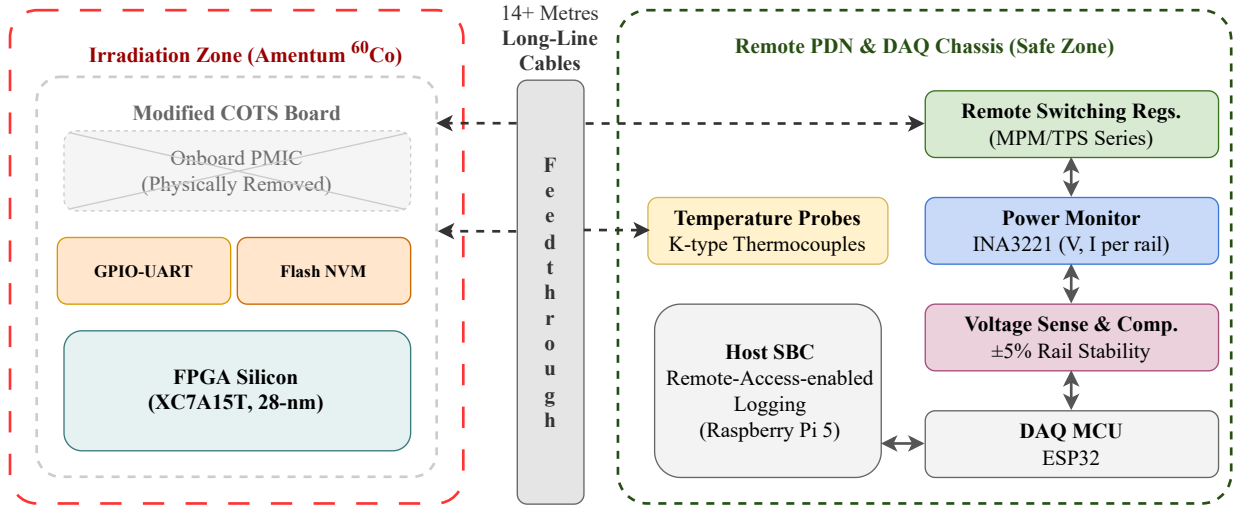


Fig. 1: Overview of the remote PDN irradiation setup. The TE0725 DUT (onboard PMICs removed) is located inside the Amentum ^{60}Co irradiation chamber. All power rails and telemetry lines are routed via 14m shielded cables through the chamber feedthrough to the external PDN and data acquisition station, which houses the custom regulator PCBs, INA3221 monitors, and host logger.

families). Voltage drops across the transmission lines were calculated in advance and compensated at the regulator outputs. Additionally, thicker cabling was selected relative to our prior campaigns [12] to minimize resistive drop over the extended cable run. Furthermore, rail voltages were verified to remain within the $\pm 5\%$ tolerance specified in the AMD 7-series datasheet throughout the experiment [13]. Moreover, the INA3221 three-channel shunt monitors on the external PCBs provided continuous logging of per-rail voltage and current. A conceptual overview of the setup is illustrated in Fig. 1. In-situ current monitoring via the INA3221 provides continuous visibility of per-rail power consumption, enabling observation of radiation-induced leakage accumulation trends even after telemetry loss.

C. Irradiation Facility and Dosimetry

Irradiation was performed at Amentum’s ^{60}Co Irradiation Facility in Oxfordshire, UK. The source emits 1.25 MeV gamma photons. The experiment ran spanning 93.6 hours of continuous exposure with a single 40-minute service interruption that took place after 26.7 hours since irradiation started, which is considered negligible for annealing purposes given the cumulative dose that had already been accumulated at that point.

The dose rate was $1.2\text{ Gy/min} \pm 10\%$, yielding a TID of $6,680\text{ Gy} \pm 10\%$ as certified by Amentum using instrumentation calibrated to national standards (Table I). This dose rate is approximately $7\times$ to $24\times$ lower than the high-rate ^{60}Co campaigns reported in our prior work (under review) [12], placing this experiment in a domain highly relevant to evaluating system-level behavior under low-dose-rate conditions, though definitive ELDRS parametric verification still requires multi-dose-rate device-level comparisons.

TABLE I: Experimental Configuration Summary

Parameter	Value
Facility	Amentum ^{60}Co Facility, Harwell, UK
Radiation source	^{60}Co , 1.25 MeV gamma
Duration	93.6 hours (near-continuous)
Service interruption	40 min (26.7 h after initiating; negligible)
Dose rate	$1.2\text{ Gy/min} \pm 10\%$
Total TID	$6,680\text{ Gy} \pm 10\%$
Device Under Test	Trenz TE0725 (Artix-7 XC7A15T, 28-nm)
Onboard PMICs	Physically removed
Local shielding	None
PDN cable length	14 m
Active during irradiation	Yes (multi-core MatMul benchmark)

D. Monitoring and Telemetry

Telemetry was obtained via three complementary channels:

- 1. UART telemetry (internal):** The embedded Triple-Core MicroBlaze subsystem transmitted CSV-formatted health packets (die temperature, rail voltages, matrix-multiplication latency, BRAM integrity flag, clock frequency) via UART until signal loss.
- 2. INA3221 (external):** Per-rail current and voltage were logged continuously on the external PDN PCBs throughout the full 93.6-hour run, providing an independent view of FPGA power consumption after UART loss.
- 3. Post-irradiation diagnostics:** Following extraction from the irradiator, the DUT was connected via JTAG to AMD Vivado Hardware Manager to assess fabric reconfigurability

and retrieve live XADC readings (die temperature and supply-rail voltages).

IV. RESULTS AND OBSERVATIONS

A. UART Telemetry and Peripheral Failure

Internal UART telemetry was received and logged until the accumulated TID reached approximately 540 Gy (corresponding to 7.5 hours of irradiation at 1.2 Gy/min). At this point, communication failed abruptly due to TID-induced parametric degradation in the FPGA's I/O circuitry supplied by V_{CCIO} . Cumulative radiation reduced the output driver strength and narrowed the voltage margins. Consequently, the weakened drivers could no longer maintain signal integrity across the highly capacitive 14 m cable, dropping the UART signals below valid logic thresholds at the receiver. The V_{CCINT} rail remained unaffected, as evidenced by its steady, nominal current draw.

Crucially, external INA3221 monitoring confirmed that current consumption on all power rails remained nominal after the UART loss, indicating that the FPGA core continued to draw power and operate despite the communication peripheral failure.

It is notable that the UART communication loss threshold observed here (≈ 540 Gy) is substantially higher, by approximately $7\times$ in cumulative dose, than the $\approx 76\text{--}78.5$ Gy transceiver-driven communication failures observed in our prior high-rate ^{60}Co and ^{137}Cs campaigns using standard onboard commercial bridges [12]. This indicates that routing a soft AXI UARTlite interface directly through a GPIO output buffer over extended lines can substantially raise the UART telemetry loss threshold, though it is acknowledged that the lower dose rate in this campaign is a confounding factor and the two effects cannot be fully decoupled without a dedicated controlled comparison.

Following UART loss at ≈ 540 Gy, the health of the device was tracked exclusively through the INA3221 external rail

monitors. Current consumption on the peripheral I/O rails ($3.3\text{ V } V_{CCIO}$ and $1.8\text{ V } V_{CCAUX}$) exhibited a gradual positive drift over the remainder of the 93.6-hour run, which is qualitatively consistent with TID-induced sub-threshold leakage accumulation in higher-voltage oxide structures. The $1.0\text{ V } V_{CCINT}$ core rail remained comparatively stable throughout. Full quantitative analysis of the rail current progression is deferred to a near-future planned journal submission.

B. Post-Irradiation Diagnostics

Following extraction from the irradiation chamber, the DUT underwent a structured post-irradiation diagnostic sequence:

- **JTAG reconfigurability:** The TE0725 was connected to a host PC via JTAG, and the Vivado Hardware Manager successfully detected the Artix-7 device in the JTAG chain. The multi-core MicroBlaze benchmark bitstream was then programmed directly via JTAG, and the device accepted configuration without error (Fig. 2). Successful JTAG programming confirms that the JTAG TAP controller, configuration memory cells, and core LUT-interconnect fabric of the 28-nm silicon remained fully operational.
- **XADC readings:** With the benchmark bitstream loaded, live XADC readings of die temperature and supply-rail voltages (V_{CCINT} , V_{CCAUX} , V_{CCBRAM}) were retrieved through the Vivado Hardware Manager. These readings were consistent with the pre-irradiation baseline measurements recorded at our laboratory before the Harwell campaign, with no anomalous voltage or temperature offset detected.
- **Flash memory:** The QSPI flash memory device failed to reconfigure the FPGA autonomously upon power-up, indicating permanent damage to the non-volatile memory. This failure is consistent with the known vulnerability of QSPI flash devices to accumulated TID at this dose level, as also reported in our prior studies in previous campaigns [12]. The failure of the flash does not affect the FPGA fabric itself, which can be reconfigured via JTAG for continued operational use.

A summary of key experimental parameters is provided in Table I, and a comparison against selected published studies is provided in Table II.

V. COMPARATIVE ANALYSIS

Table II places this work in the context of representative studies on Artix-7 and comparable 28-nm COTS FPGA platforms. Several distinctions are worth highlighting.

First, the majority of published campaigns irradiate boards at high dose rates ($>5\text{ Gy/min}$) for practical time constraints. This work, at 1.2 Gy/min over 93.6 hours, is among the longest duration continuously powered COTS FPGA irradiation campaigns reported to date, and the dose rate falls within an intermediate regime relevant to dose-rate effects, though a complete ELDRS parametric assessment requires a dedicated multi-rate comparison.

Second, and most critically from a survivability perspective, Hu et al. [11] irradiated Artix-7 boards (28-nm) with ^{60}Co at comparable dose rates but applied lead shielding to

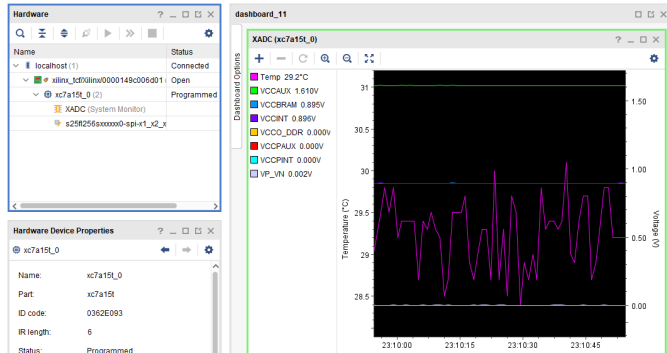


Fig. 2: Post-irradiation Vivado Hardware Manager screenshot showing (left) successful JTAG detection of the TE0725 Artix-7 XC7A15T and completed bitstream programming after 6,680 Gy total dose; and (right) live XADC dashboard confirming on-chip die temperature and supply-rail voltage readings consistent with pre-irradiation baselines.

TABLE II: Comparative Summary of Selected COTS FPGA Gamma Irradiation Studies

Study	Device (node)	Source	Dose rate	Max TID	Duration	Powered	Shielded	Outcome
West et al. [3]	COTS SBC	^{60}Co	8.16–33.6 Gy/min	111.1 $\pm$ 5.5 Gy	3–14 min	Yes	No	PMIC failure
Liu et al. [6]	Anti-fuse FPGA	^{60}Co	0.16–10.26 Gy/min	334 Gy (LDR)	0.27–34.6 h	Yes	Yes (driver module)	LDR doubles threshold
Gao et al. [7]	SRAM FPGA	^{60}Co	0.468–42.6 Gy/min	2.5 kGy (LDR)	0.82–89 h	Biased	Yes	LDR > HDR tolerance
Bricas et al. [9]	Artix-7/Spartan-7 (28-nm) Cyclone-10LP (60-nm)	X-ray	6.98 Gy/min	3.56 kGy	8.5 h	Yes	Yes	No failure; delay speedup
Vartanian et al. [10]	Kintex UltraScale	^{60}Co 2 MeV e^-	2.4 Gy/min 44.1–58.2 Gy/min	6.2 kGy 50 kGy	14.3–43.1 h	Yes	Yes	No failure
Hu et al. [11]	Artix-7 (28-nm)	^{60}Co	0.33–1.45 Gy/min	6.26 kGy	23–72 h	Yes	Yes (LDO)	LDO and FPGA failure
Al-Hasan et al.* [12]	Artix-7 (28-nm)	$^{137}\text{Cs}/^{60}\text{Co}$	8.34–28.2 Gy/min	$\approx$ 8 kGy	0.1–15 h	Yes	No (remote PDN)	Silicon intact; UART failed at 76 Gy
This work	Artix-7 (28-nm)	^{60}Co	1.2 Gy/min	6,680 Gy$\pm$10%	93.6 h	Yes	No (remote PDN)	Silicon intact; flash failed; UART failed at 540 Gy

*Our own work [Under Review]. LDR: Low Dose Rate; HDR: High Dose Rate; SBC: Single Board Computer; PDN: Power Delivery Network.

the onboard LDOs to extend their operational life, reaching ≈ 6 kGy before system-level failure. The present work exceeds this threshold (6,680 Gy $\pm 10\%$) without any local shielding, relying solely on remote power delivery over a 14 m cable run.

Third, devices in many published studies are either unbiased during irradiation or only statistically biased [6], [7], whereas in this work, the FPGA was actively executing a computational benchmark throughout, thus constituting a stricter and operationally more representative test condition.

Together, these observations suggest that a remote PDN strategy, even without physical shielding, can sustain a 28-nm COTS FPGA through gamma doses exceeding those achievable with shielded onboard regulation, while simultaneously providing a more representative active-operation test setting.

VI. CONCLUSION

This paper has reported a 93.6-hour, near-continuous ^{60}Co irradiation of a remotely powered Trenz Electronic TE0725 COTS FPGA board at Amentum’s Harwell facility, reaching a cumulative TID of 6,680 Gy $\pm 10\%$ at a dose rate of 1.2 Gy/min. The Artix-7 XC7A15T silicon fabric survived the full exposure: post-irradiation JTAG reconfiguration succeeded, on-chip XADC readings were consistent with pre-irradiation baselines, and no permanent damage to the core logic fabric was detected. The QSPI flash memory failed, which prevented autonomous boot. Also, the GPIO-mapped soft UART link failed at approximately 540 Gy, which is a threshold markedly higher than the commercial transceiver failures observed in prior high-rate campaigns, demonstrating the utility of simplified peripheral routing.

This result extends the demonstrated survivable TID of a remotely powered 28-nm COTS FPGA beyond the ≈ 6 kGy reported for a shielded onboard-regulated architecture [11], reinforcing remote power delivery as an effective and low-cost approach for deploying COTS FPGAs in sustained gamma radiation environments. The dose rate employed here also underscores the importance of long-duration, low-rate cam-

paigns for realistic assessment of COTS electronics intended for nuclear decommissioning robotics.

A limitation of this study is the lack of microscopic defect isolation within the degraded I/O blocks and the absence of concurrent high-dose-rate cross-testing. To address this, a comprehensive quantitative analysis tracking continuous rail current drift trends, dynamic leakage accumulation, and recovery annealing profiles is currently in draft for a peer-reviewed journal submission. Future work will target even lower dose rates to map the full ELDRS response of 28-nm COTS FPGA platforms, and will evaluate the integration of radiation-tolerant components within the remote PDN to extend telemetry chain survivability and use them as features for early fault detection to enhance predictive maintenance of electronics in harsh environments. This will expand upon our previous generative frameworks developed to counter radiation-induced sensor data scarcity via adversarial data synthesis [14].

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